DLD - Theory - 13

5/3/24

Design a 4 bit odd number detector circuit.

Truth table:

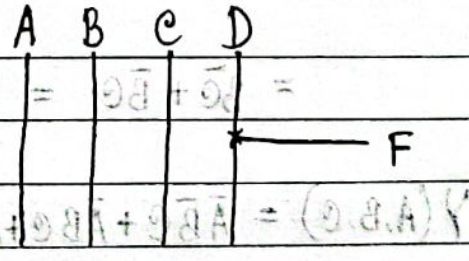
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	1	1	1	1
1	1	0	0	0
1	1	0	1	1
1	0	1	0	0
1	0	1	1	1
0	0	0	0	0
0	1	0	1	
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	1	1	1	1

$F(A,B,C,D) = \bar{A}\bar{B}\bar{C}D + \bar{A}BCD + AB\bar{C}D + A\bar{B}CD$

$+ \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C}D + ABCD.$

AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

Simplified function $F(A,B,C,D) = D$



Design a 3 bit 2's compliment genarator circuit.

Truth table:

A	B	C	W	X	Y
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

AB \ C	0	1
00		1
01	1	1
11		
10	1	

00	1
01	1
11	1
10	1

$W(A,B,C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$

$= \bar{A}C + \bar{A}B + A\bar{B}\bar{C}$

00	1
01	1
11	1
10	1

$X(A,B,C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C$

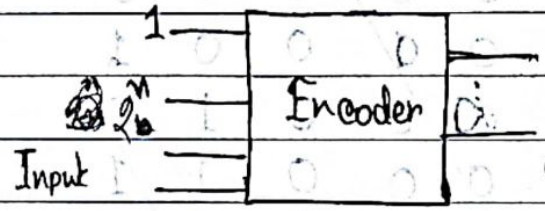
$= B\bar{C} + \bar{B}C = B \oplus C$

$Y(A,B,C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$

$= C$

Encoder: An encoder is a digital circuit that has 2^n input lines & n number of output line. It produces binary equivalent of the input.

4 to 2 encoder

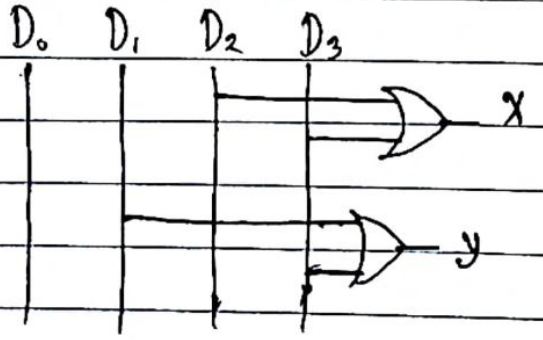


(Only on terms)

D_0	D_1	D_2	D_3	x	y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

$x = D_2 + D_3$

$y = D_1 + D_3$



DLD - Theory - 14

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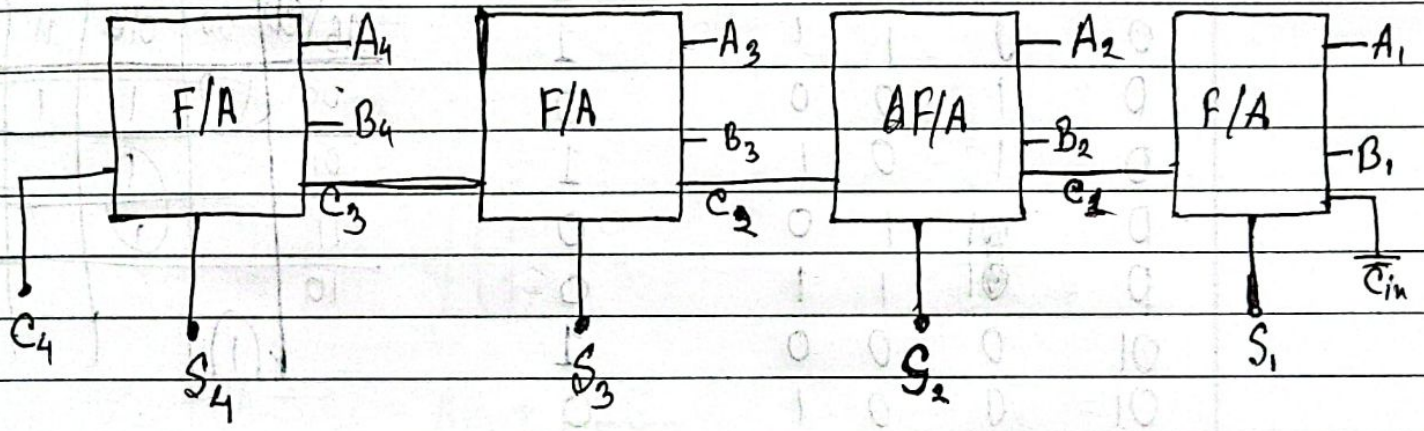
Design a combination logic circuit to solve the problem:

$$\begin{array}{cccc} A_4 & A_3 & A_2 & A_1 \\ +\ B_4 & B_3 & B_2 & B_1 \\ \hline C_4 & S_4 & S_3 & S_2 \quad S_1 \end{array}$$



$S_1 = A_1 \oplus B_1 \oplus C_{in}$ $\quad C_1 = C_{in}(A_1 \oplus B_1) + A_1 B_1$

$S_2 = A_2 \oplus B_2 \oplus C_{in}$ $\quad C_2 = C_{in}(A_2 \oplus B_2) + A_2 B_2$

$S_3 = A_3 \oplus B_3 \oplus C_2$ $\quad C_3 = C_2(A_3 \oplus B_3) + A_3 B_3$

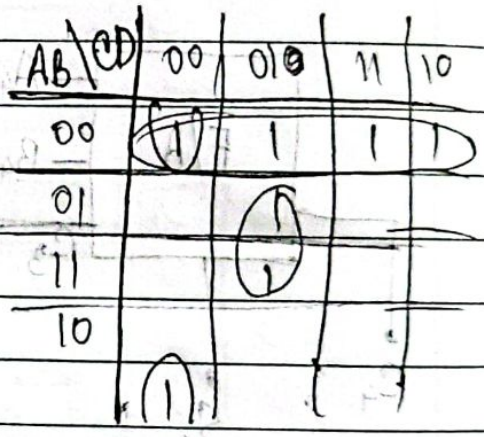
$S_4 = A_4 \oplus B_4 \oplus C_3$ $\quad C_4 = C_3(A_4 \oplus B_4) + A_4 B_4$

$S = A \oplus B \oplus C_{in}$

$C = C_{in}(A \oplus B) + AB$

Design a fibonacci number detector that can detect fibonacci number up to 15

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



$F(A,B,C,D) = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$

$+ AB\bar{C}D$

$= \bar{A}\bar{B} + B\bar{C}D + \bar{B}\bar{C}\bar{D}$

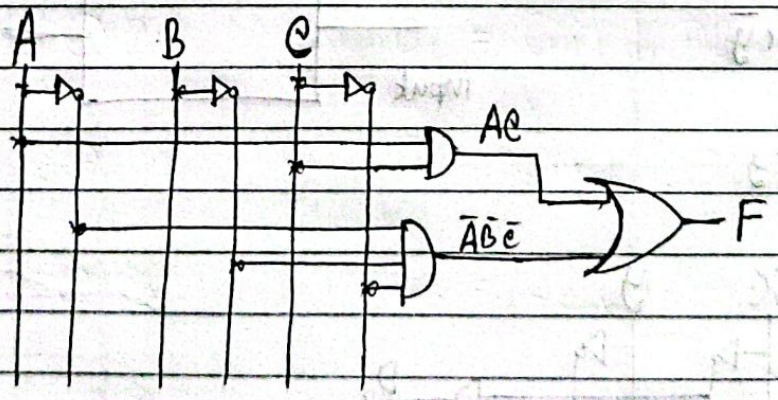
Design an elevator circuit for a 7th floor building which will stop at ground, 5th and top floor only.

$$F(A,B,C) = \Sigma_m(0, 5, 7)$$

$$= \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$$

AB \ C	0	1
00	(1)	
01		
11		(1)
10		(1)

$$\therefore F(A,B,C) = AC + \bar{A}\bar{B}\bar{C}$$



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Decoder: A decoder is a combination circuit that converts binary information from 'n' input lines to maximum of 2^n output lines

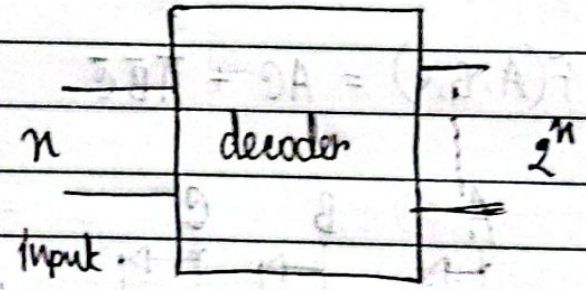
X	y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

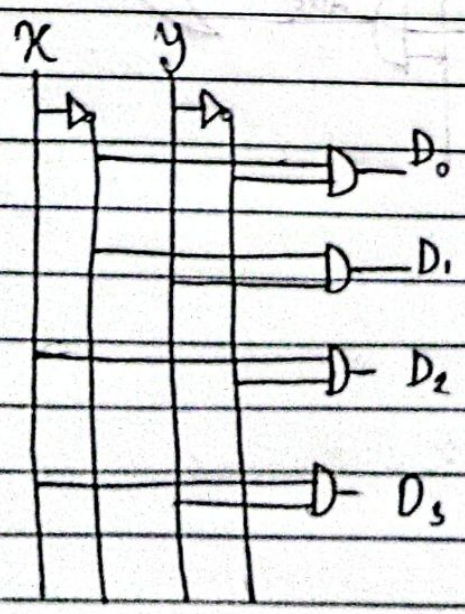
$D_0 = \bar{x}\,\bar{y}$

$D_1 = \bar{x}\,y$

$D_2 = x\,\bar{y}$

$D_3 = xy$

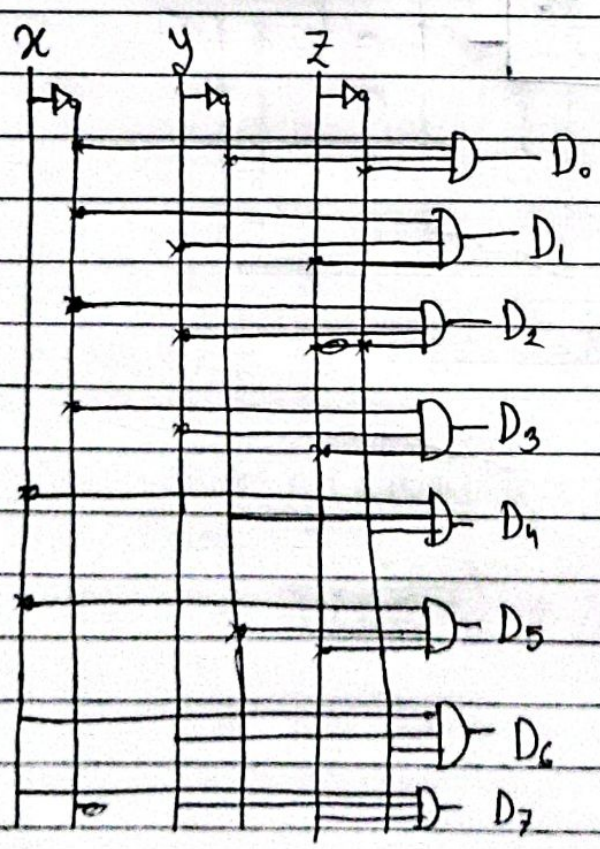


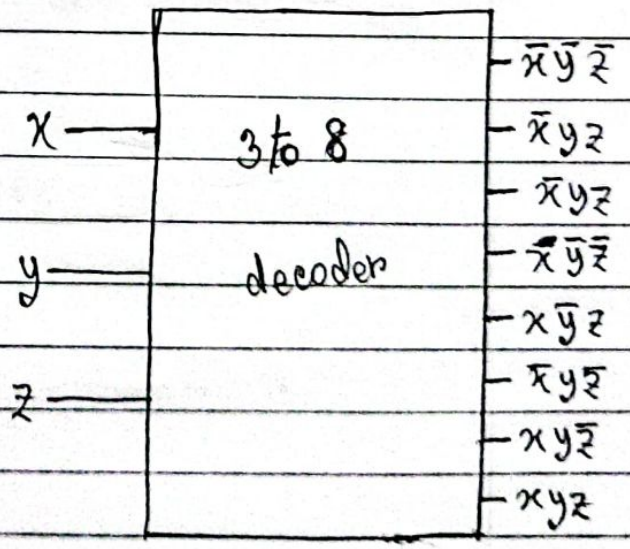


Design a 3 to 8 Decoder :

Truth table:

x	y	z	F	
0	0	0	D_0	$D_0 = \bar{x}\bar{y}\bar{z}$
0	0	1	D_1	$D_1 = \bar{x}\bar{y}z$
0	1	0	D_2	$D_2 = \bar{x}y\bar{z}$
0	1	1	D_3	$D_3 = \bar{x}yz$
1	0	0	D_4	$D_4 = x\bar{y}\bar{z}$
1	0	1	D_5	$D_5 = x\bar{y}z$
1	1	0	D_6	$D_6 = xy\bar{z}$
1	1	1	D_7	$D_7 = xyz$

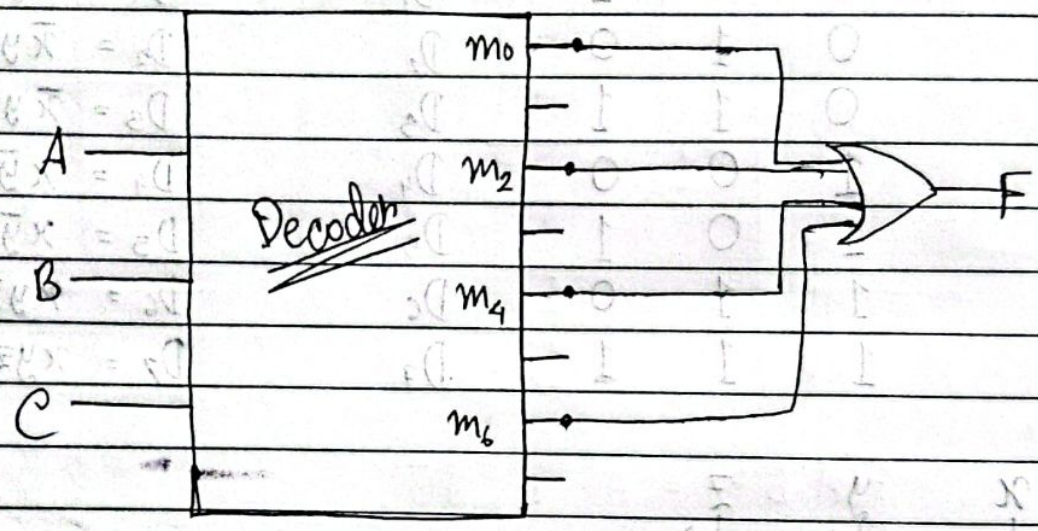




Design a 3 bit even number detector circuit using decoder

$$F(A,B,C) = \Sigma_m (0, 2, 4, 6)$$

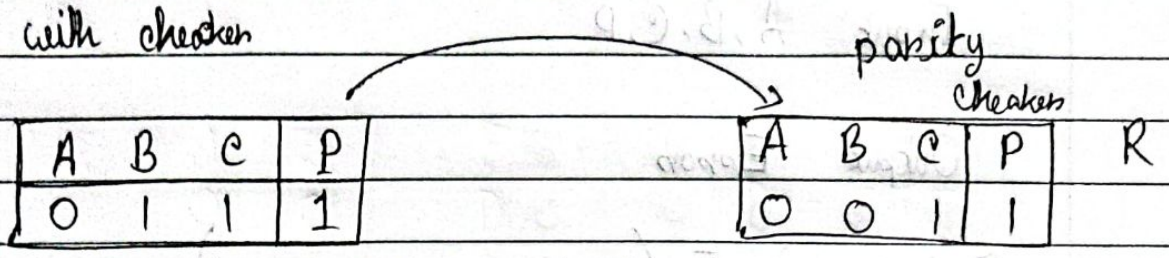
$$= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$$



DLD Lab-8

10/3/24

Experiment No 6 To. implement a 3 bit **odd parity** generator circuit. with checker



TT:

A	B	C	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$$P(A,B,C) = \bar{A}B\bar{C} + \bar{A}\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}(\bar{B}\bar{C} + BC) + A(\bar{B}C + B\bar{C})$$

$$= \bar{A}\overline{(B \oplus C)} + A(B \oplus C)$$

$$= \overline{A \oplus B \oplus C}$$

For error checker,

Input A, B, C, P

Output Error.

$$E(A, B, C, D) = \Sigma_m(0, 3, 5, 6, 9, 10, 12, 15)$$

Decoder

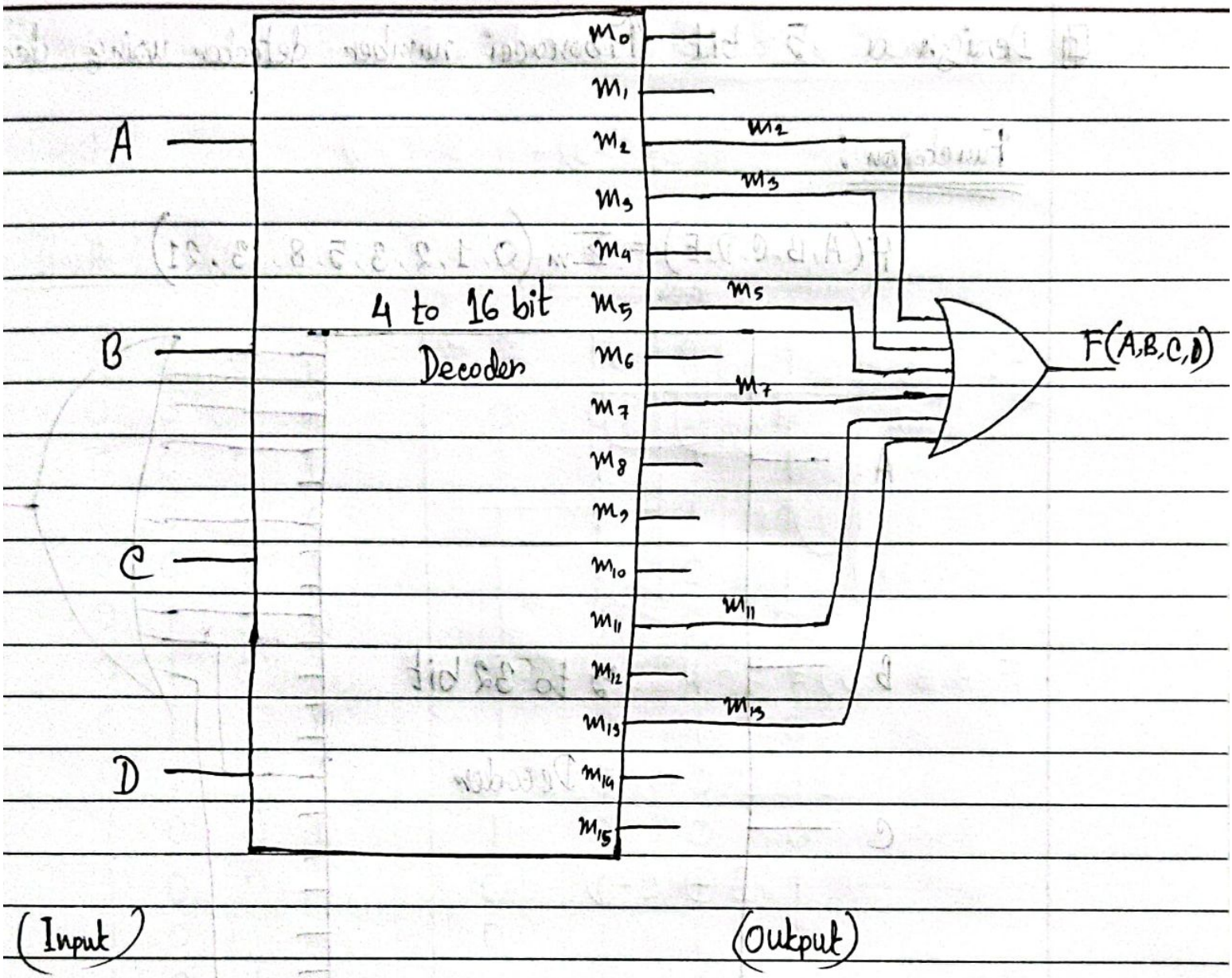
* Implement a 4 bit prime number detector using decoder.

Truth table :

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

$F(A,B,C,D) = \Sigma_m(2, 3, 5, 7, 11, 13)$

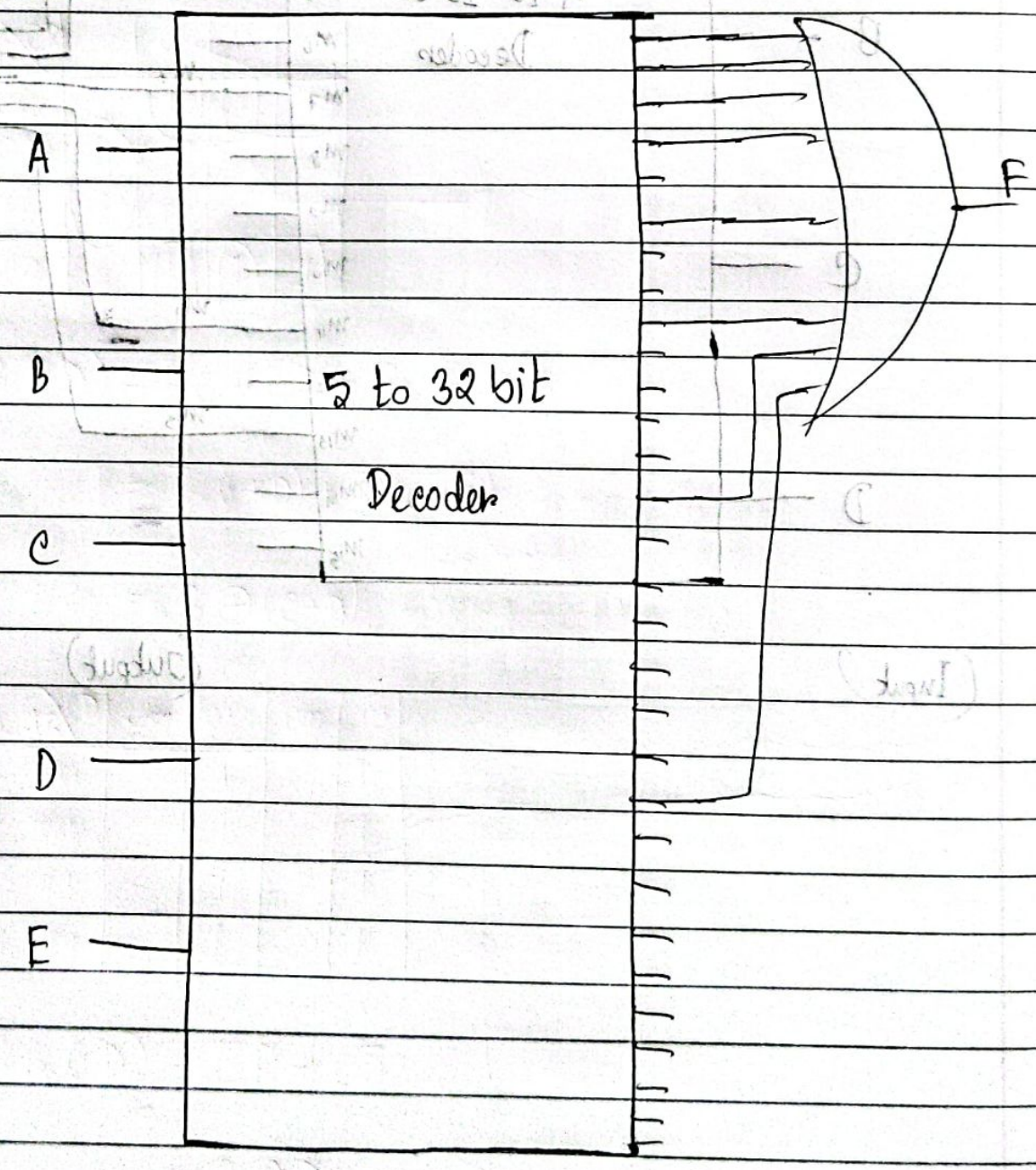
To implement a 4 bit prime number detector we need 4 to 16 bit decoder.


A
B
C
D
4 to 16 bit
Decoder
m_0
m_1
m_2
m_3
m_4
m_5
m_6
m_7
m_8
m_9
m_{10}
m_{11}
m_{12}
m_{13}
m_{14}
m_{15}
F(A,B,C,D)
(Input)
(Output)

Design a 5 bit Fibonacci number detector using decoder.

Function:

$$F(A,B,C,D,E) = \sum_m (0,1,2,3,5,8,13,21)$$



DLD Lab-8

24/03/24

Experiment No 7 | To implement a 4 bit 2's compliment generator circuit.

Truth table:

A	B	C	D	→	E	F	G	H
					2's compliment			
0	0	0	0		0	0	0	0
0	0	0	1		1	1	1	1
0	0	1	0		1	1	1	0
0	0	1	1		1	1	0	1
0	1	0	0		1	1	0	0
0	1	0	1		1	0	1	1
0	1	1	0		1	0	1	0
0	1	1	1		1	0	0	1
1	0	0	0		1	0	0	0
1	0	0	1		0	1	1	1
1	0	1	0		0	1	1	0
1	0	1	1		0	1	0	1
1	1	0	0		0	1	0	0
1	1	0	1		0	1	0	1
1	1	1	0		0	1	1	0
1	1	1	1		0	1	0	1

E:

AB \ CD	00	01	11	10
00		1	1	1
01	1	1	1	1
11				
10	1			

$$E(A,B,C,D) = \bar{A}C + \bar{A}D + \bar{A}B\bar{C} + AB\bar{C}\bar{D}$$

$$= \bar{A}(C + B\bar{C}) + \bar{A}D + AB\bar{C}\bar{D}$$

$$= \bar{A}(\bar{C} + B) + \bar{A}D + AB\bar{C}\bar{D}$$

$$= \bar{A}(C + B + D) + AB\bar{C}\bar{D}$$

$$\therefore E(A,B,C,D) = \bar{A}(B+C+D) + A\bar{B}\bar{C}\bar{D}$$

$$= \bar{A}(B+C+D) + A\overline{(B+C+D)}$$

$$= A \oplus (B+C+D)$$

F:

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	1			
10		1	1	1

$$F(A,B,C,D) = \bar{B}C + \bar{B}D + B\bar{C}\bar{D}$$

$$= \bar{B}(C+D) + B\overline{(C+D)}$$

$$= B \oplus (C+D)$$

G:

AB \ CD	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

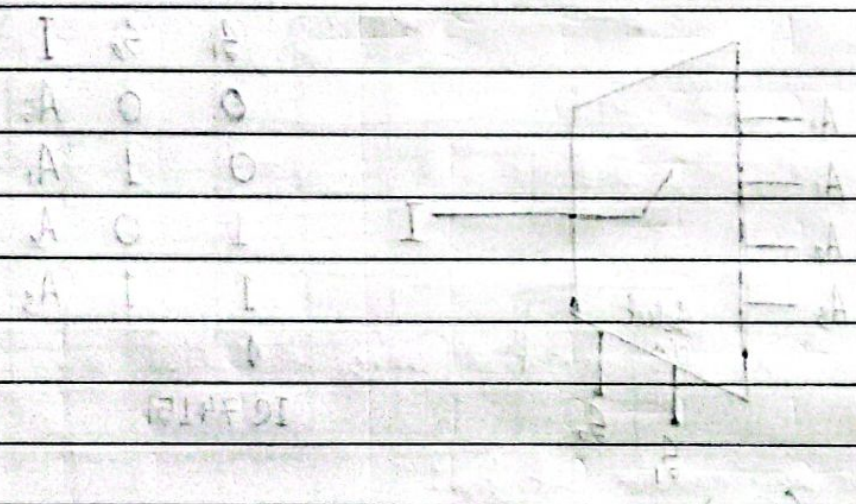
$$G(A,B,C,D) = \bar{C}D + C\bar{D}$$

$$= C \oplus D$$

H :

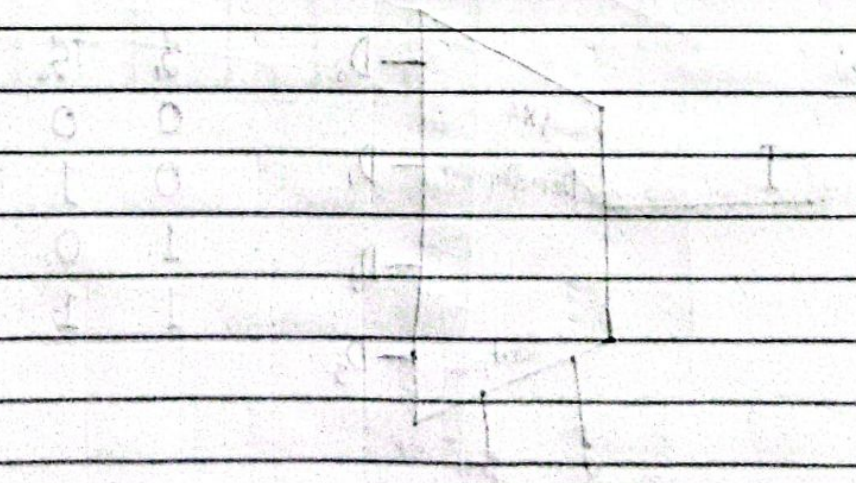
AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

$H(A,B,C,D) = \cancel{\bar{C}\bar{D} + C\bar{D}}\ D$



$$I\ (\quad) = \bar{S}_3\bar{S}_2\bar{A}_3 + \bar{S}_3S_2A_2 + S_3\bar{S}_2A_2 + S_3S_2A_3$$

$$= 1 \cdot \bar{0}\bar{A}_2 + 0 \cdot 0 \cdot A_2 + 1 \cdot 1 A_2 + 1 \cdot 0 \cdot A_3$$



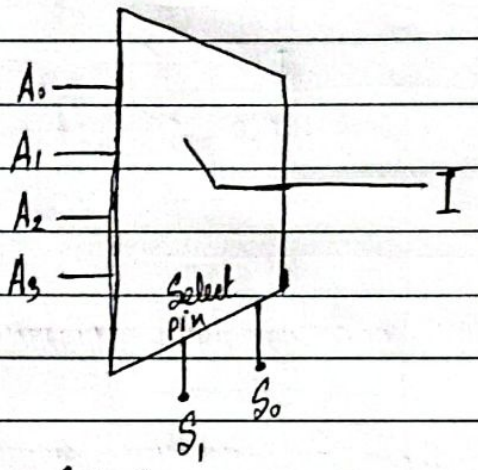
2/4/24

DLD Theory-16

3 to 8 decoder: Prime number detector -

Truth table:

* Multiplexer is always in input side.



S_1	S_0	I
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

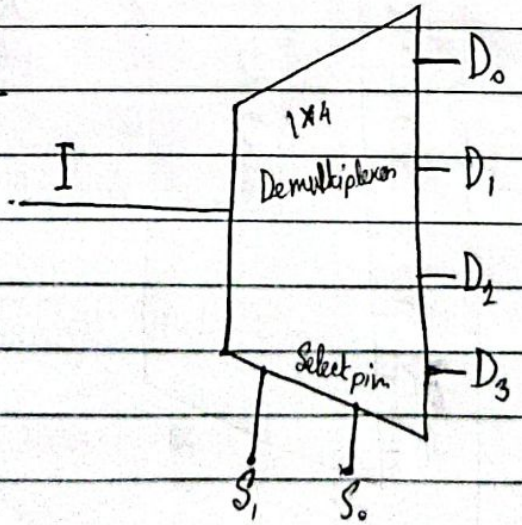
IC 74151

$$I = \overline{S_0}\,\overline{S_1}A_0 + \overline{S_1}S_0A_1 + S_1\overline{S_0}A_2 + S_1S_0A_3$$

if $S_1=1$, $S_0=0$ then, $= 1\cdot0\cdot A_0 + 0\cdot0\cdot A_1 + 1\cdot1\cdot A_2 + 1\cdot0\cdot A_3$

$= A_2$

Demultiplexer:



S_1	S_0	Y
0	0	
0	1	
1	0	
1	1	

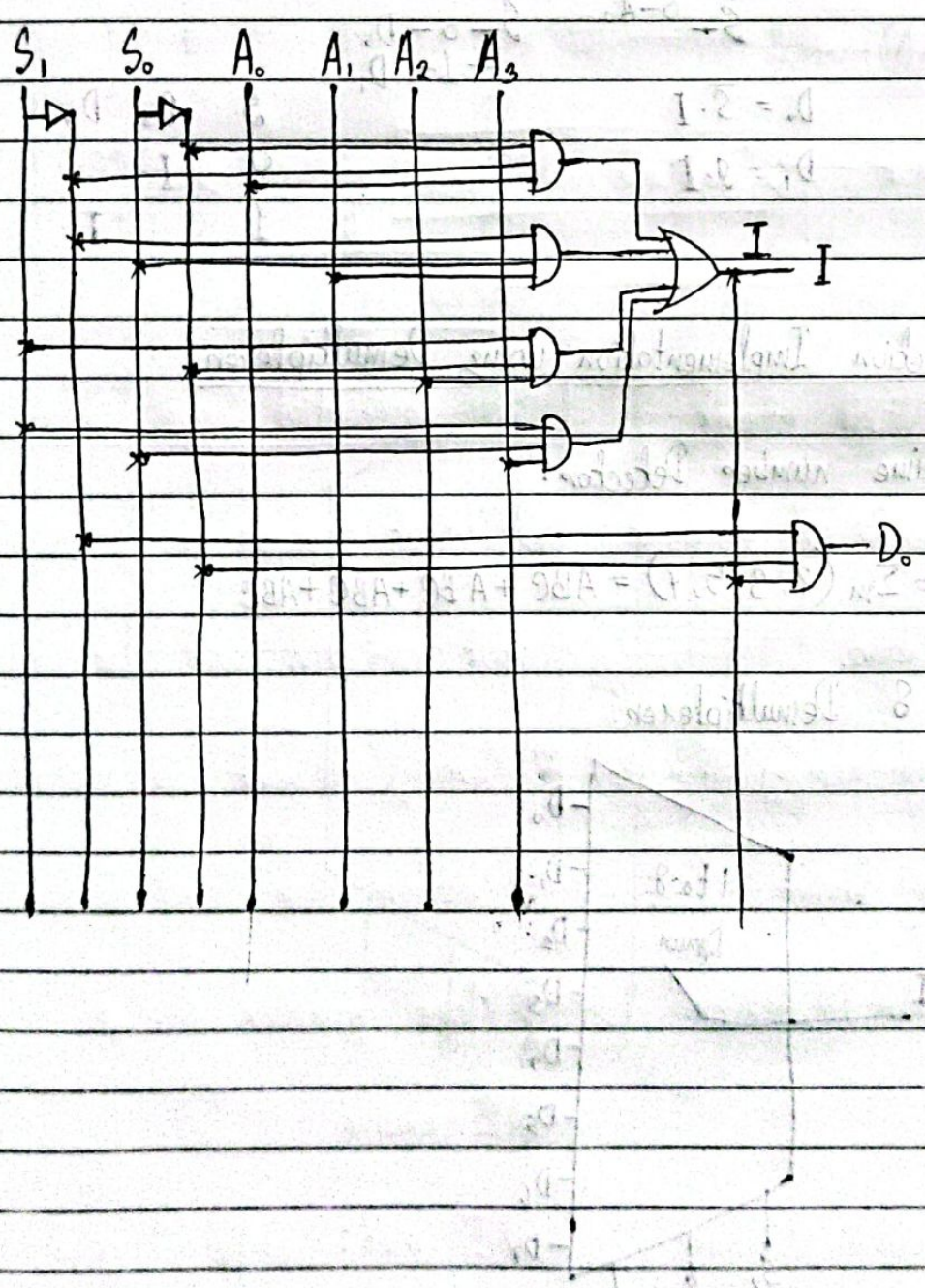
S_1	S_0	D_0	D_1	D_2	D_3
0	0	I			
0	1		I		
1	0			I	
1	1				I

$D_0 = \bar{S}_1 \bar{S}_0 I$

$D_1 = \bar{S}_0 \bar{S}_1 I$

$D_2 = S_1 \bar{S}_0 I$

$D_3 = S_1 S_0 I$



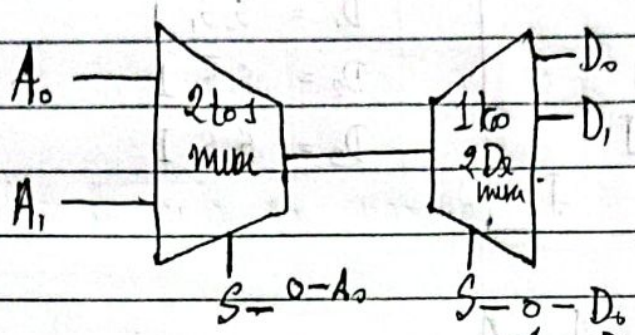
8 to 1 mux

1 to 8 mux

DLD Theory - 17

16/04/24

Multiplexer - Demultiplexer:



$D_0 = \bar{S} \cdot I$

$D_1 = S \cdot I$

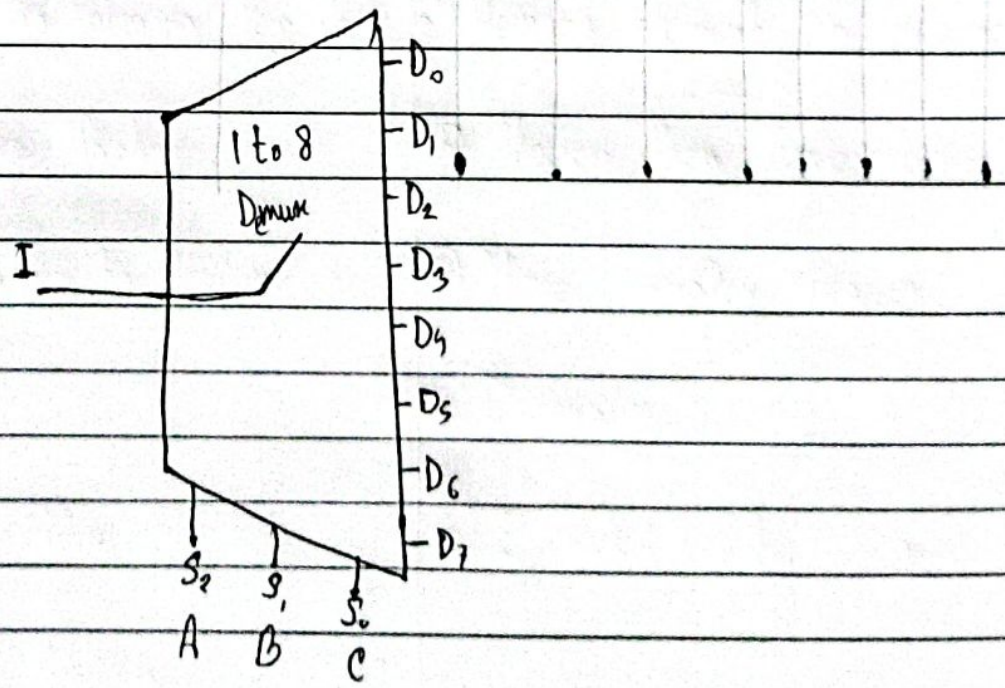
S	D_0	D_1
0	I	
1		I

Boolean function Implementation using Demultiplexer:

* 3 bit prime number Detector:

$F(A,B,C) = \Sigma_m (2,3,5,7) = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + ABC$

1 to 8 Demultiplexer:

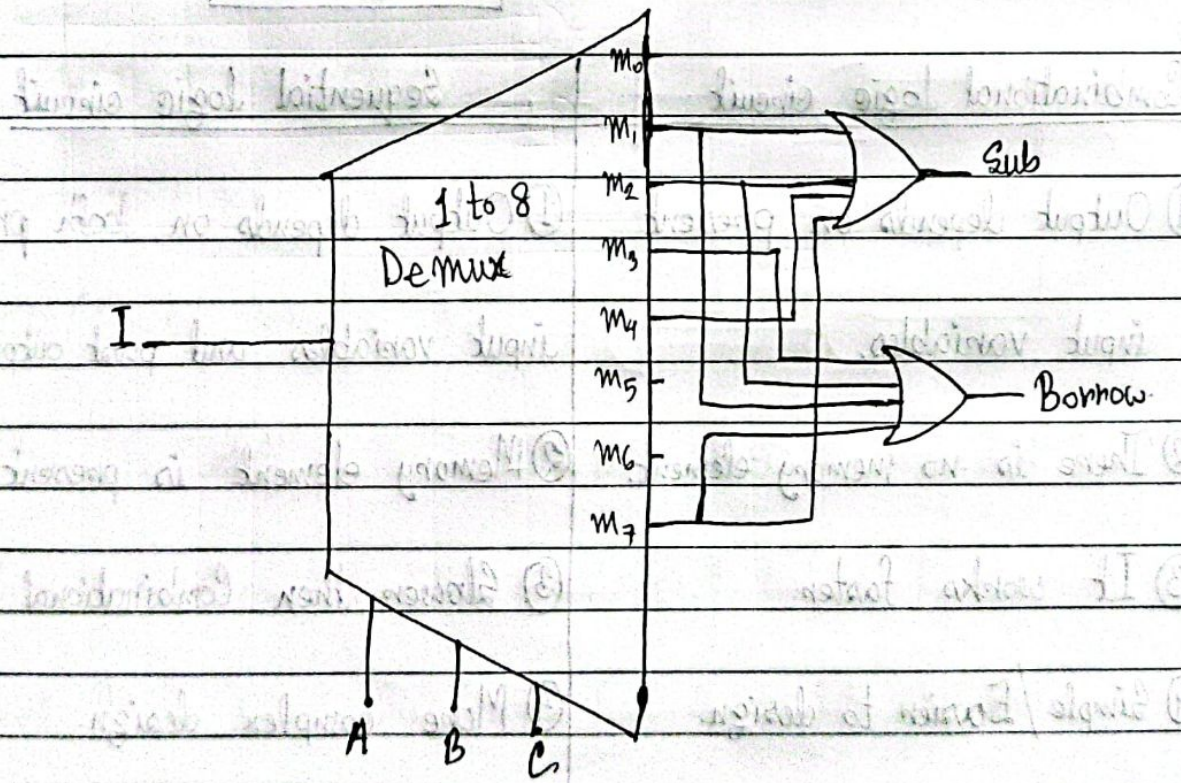


* Implementing a full subtractor using demultiplexer:

A	B	C	Sub	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

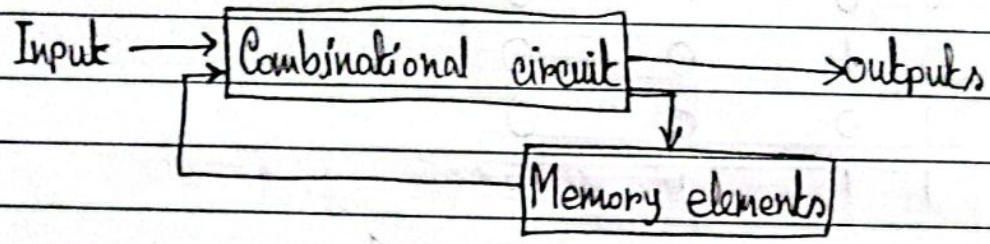
$Sub(A,B,C) = \Sigma_m(1,2,4,7)$

$Borrow(A,B,C) = \Sigma_m(1,2,3,7)$



6 Sequential Logic circuit:

Sequential logic circuit is a logical circuit in which the output depends on present input variables and past outputs.



Combinational logic circuit	Sequential logic circuit
① Output depends on present input variables.	① Output depends on both present input variables and past output var.
② There is no memory element.	② Memory element is present.
③ It works faster	③ Slower then Combinational L.C
④ Simple/Easier to design	④ More complex design
⑤ Cheaper	⑤ Expensive.
⑥ Example: Adder, Encoder, decoder, Multiplexer.	⑥ Example: Counter, Register etc.

Latch: Data Store করে, Memory element. [1 bit].

Latches are said to be **level sensitive devices**;

Flip-flops are **edge-sensitive devices.**

Latch

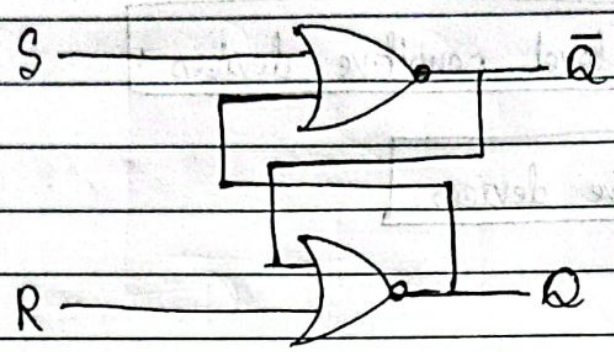
- SR Latch (Set-Reset)
- Jk Latch (Jack-kilby)
- D Latch (Data Latch)
- T Latch (Toggle Latch)

SR (Set-Reset) Latch:

The SR Latch is a circuit with two cross-coupled NOR gates or two crossed-coupled NAND gates, and two inputs labeled S for set and R for reset. The Latch has 2 useful states.

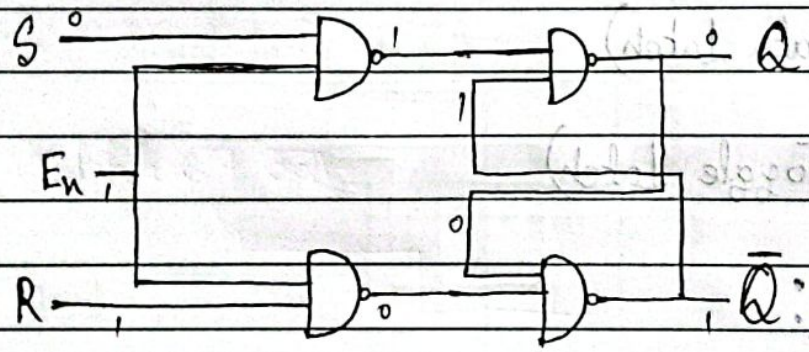
S	R	Q	$\overline{Q}$	
0	0	memory		
0	1	0	1	→ Reset condition
1	0	1	0	→ Set condition.
1	1	Ambiguous		

* Latch with Nor Gates:



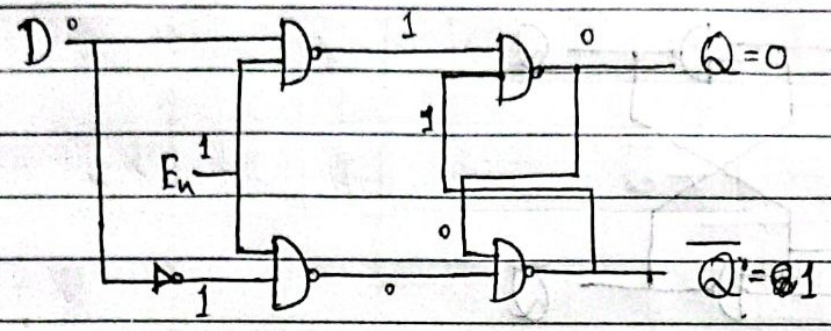
S	R	Q	$\bar{Q}$
0	0	memory	
0	1	0	1
1	0	1	0
1	1	forbidden	

* Latch with NAND Gates: E_n → Enable pin



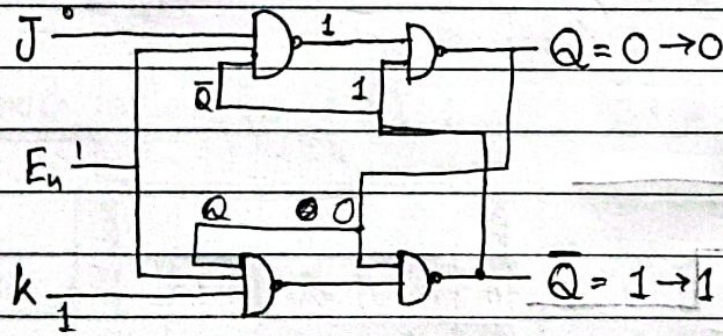
একটা Input 0 হলেই output 1.

D-Latch: Frequently used for storing data in digital systems.



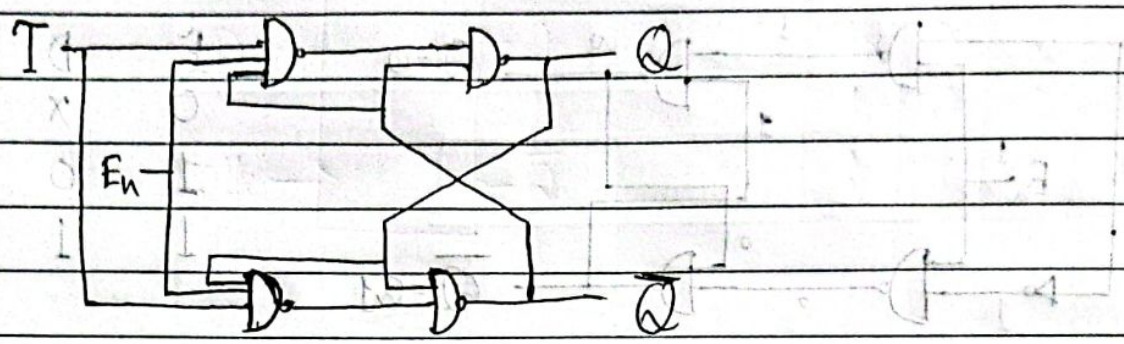
E_n	D	Q
0	x	memory/Q_0
1	0	0
1	1	1

Jk Latch: A modified version of SR Latch for removing Ambiguity.



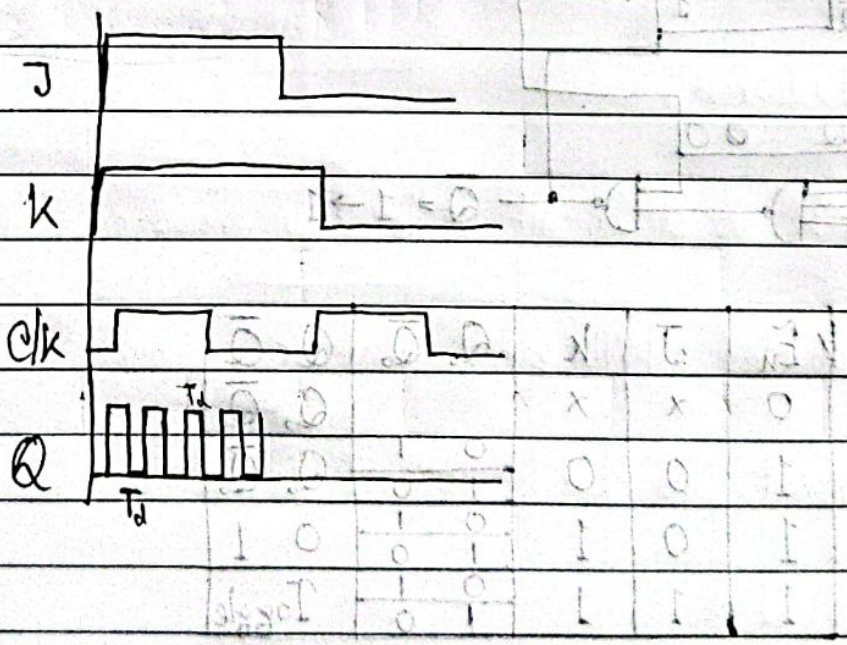
E_n	J	k	Q_0 $\bar{Q}_0$	Q $\bar{Q}$
0	x	x		Q_0 $\bar{Q}_0$
1	0	0	0 1 / 1 0	Q_0 $\bar{Q}_0$
1	0	1	0 1 / 1 0	0 1
1	1	1	0 1 / 1 0	Toggle

T Latch (Toggle):



E_n	T	Q $\bar{Q}$
0	x	memory
1	0	memory
1	1	Toggle

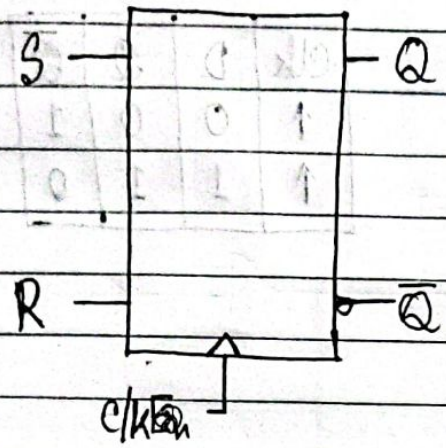
JK latch এর তরঙ্গ-

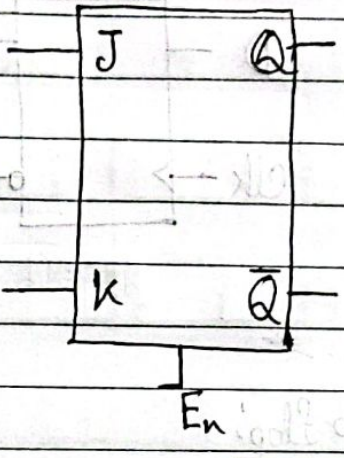


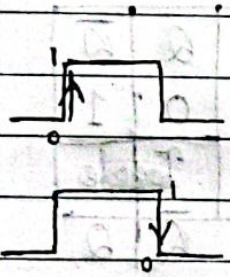
DLD Theory - 18

28/04/24

Flip-flops: Edge Sensitive device.







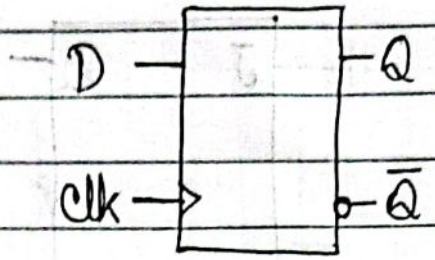
PGT: Positive Going Transition (↑)

NGT: Negative Going Transition (↓)

Truth table: for NGT:

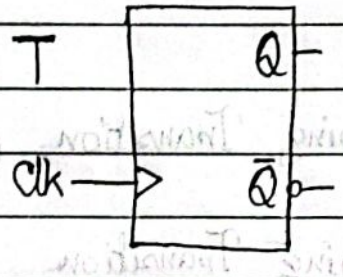
Clk	S	R	Q	$\bar{Q}$	
↓	0	0	Q_0	$\bar{Q}$	
↓	0	1	0	1	← Reset
↓	1	0	1	0	← Set
↓	1	1	Ambiguous		

D-Flip-flop:



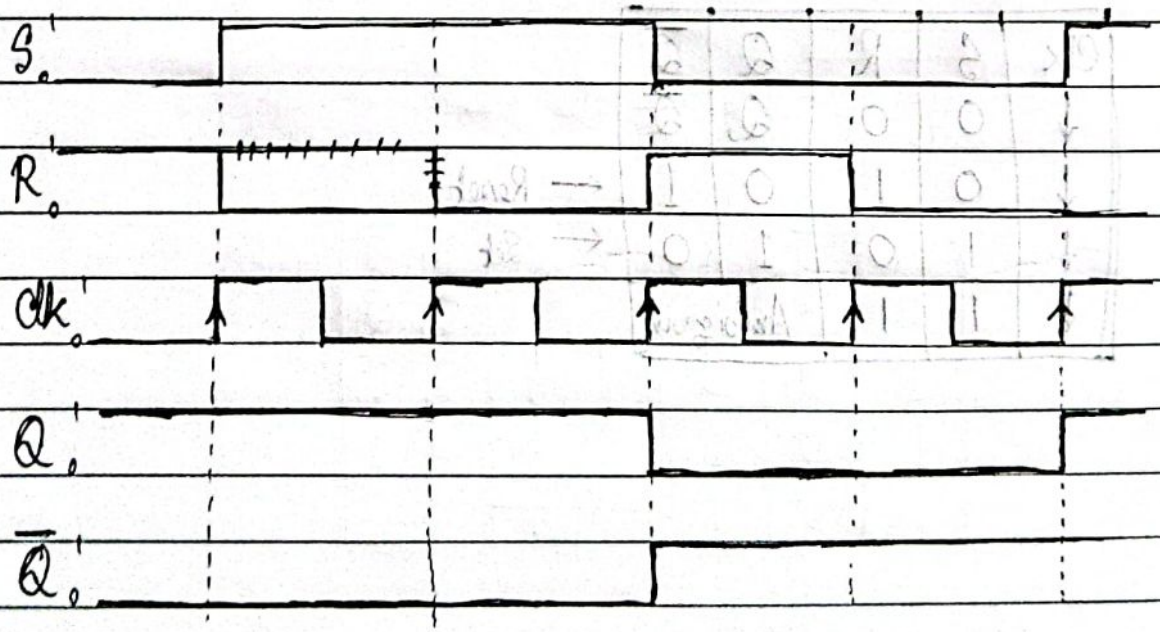
Clk	D	Q	$\bar{Q}$
↑	0	0	1
↑	1	1	0

T-Flip-flop:



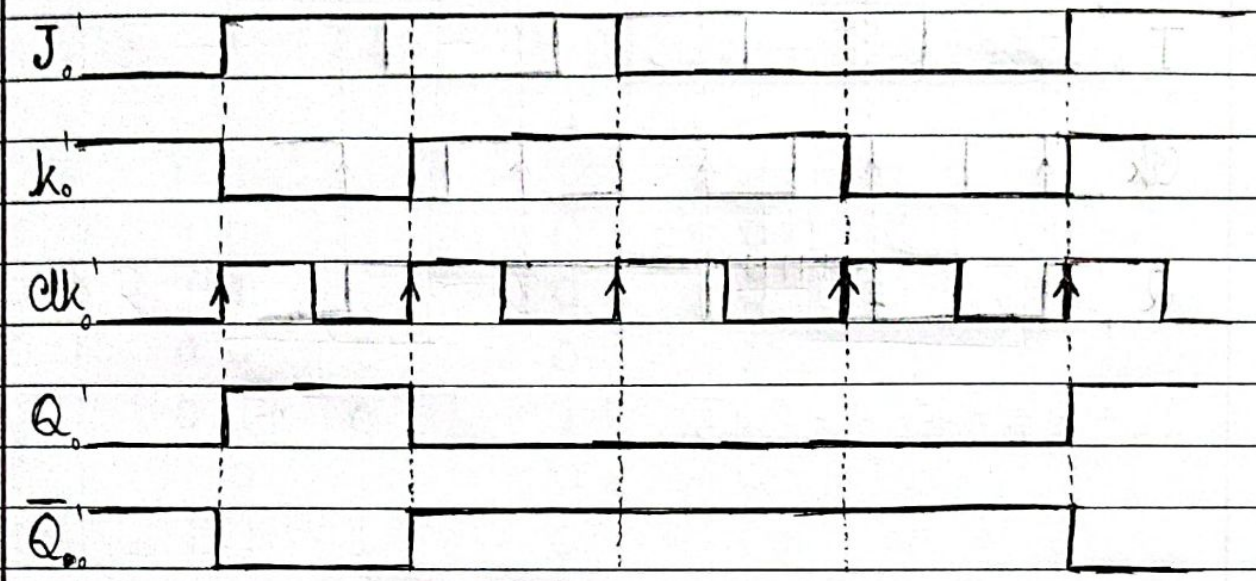
Clk	T	Q	$\bar{Q}$
↑	0	0	1
↑	1	~~Toggle~~ $\bar{Q}_0$	Q_0

Timing Diagram: (SR FF)

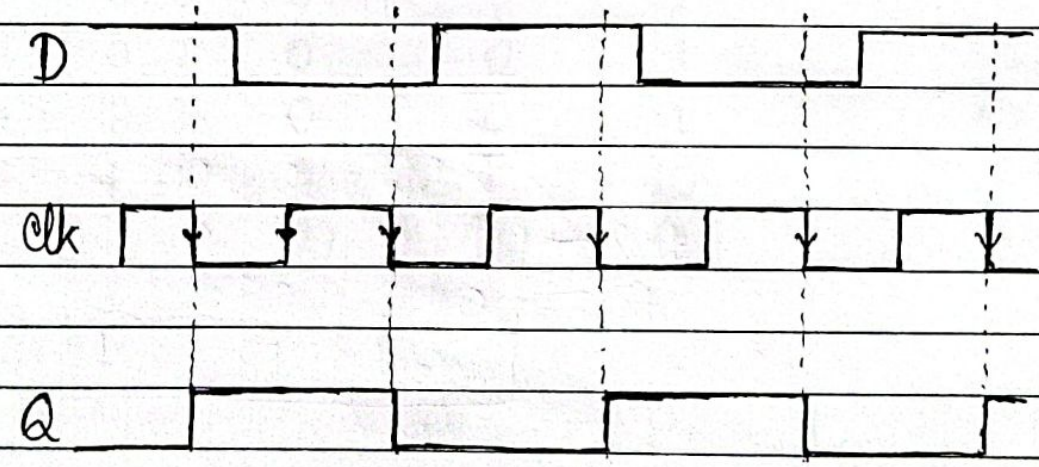


Initially, output was high.

Timing Diagram of J.k f.f:

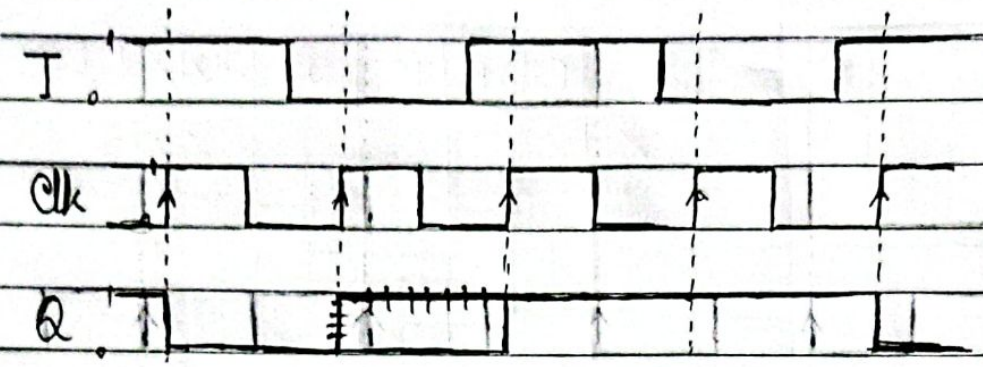


Timing diagram of D Filp-flop: (NGT)



Initially, output was Low.

Timing diagram of T-Flip-flop: (PAT)



DLD Lab-10

28/04/24

Experiment No:09 To implement a 2bit magnitude comparator.

A_1 A_0	B_1 B_0	A<B	A=B	A>B
0 0	0 0	0	1	0
0 0	0 1	1	0	0
0 0	1 0	1	0	0
0 0	1 1	1	0	0
0 1	0 0	0	0	1
0 1	0 1	0	1	0
0 1	1 0	1	0	0
0 1	1 1	1	0	0
1 0	0 0	0	0	1
1 0	0 1	0	0	1
1 0	1 0	0	1	0
1 0	1 1	1	0	0
1 1	0 0	0	0	1
1 1	0 1	0	0	1
1 1	1 0	0	0	1
1 1	1 1	0	1	0
		(Y_1)	(Y_2)	(Y_3)

$$Y_2 = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 B_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$$

$$= \bar{A}_1 \bar{B}_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) + A_1 B_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0)$$

$$= (A_0 B_0 + \bar{A}_0 \bar{B}_0)(\bar{A}_1 \bar{B}_1 + A_1 B_1)$$

$Y_1 (A<B)$:

$A_1 A_0$ \ $B_1 B_0$	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

$$Y_1 = \bar{A}_1 B_1 + \bar{A}_1 B_0 \bar{A}_0 + \bar{A}_0 B_1 B_0$$

$Y_2 (A=B)$:

$A_1 A_0$ \ $B_1 B_0$	00	01	11	10
00	1			
01		1		
11			1	
10				1

$$Y_2 = \overline{(A_0 \oplus B_0)}\ \overline{(A_1 \oplus B_1)}$$

$y_3(A>B)$:

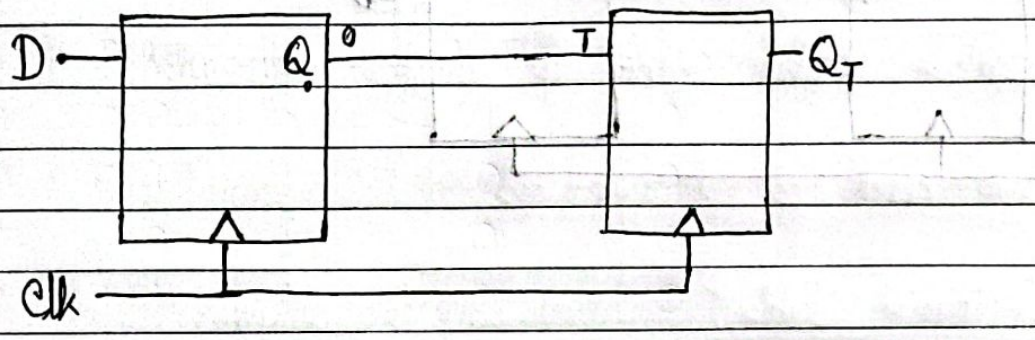
A_1A_0 \ B_1B_0	00	01	11	10
00			0	
01	1		0	
11	1	1	0	1
10	1	1	0	

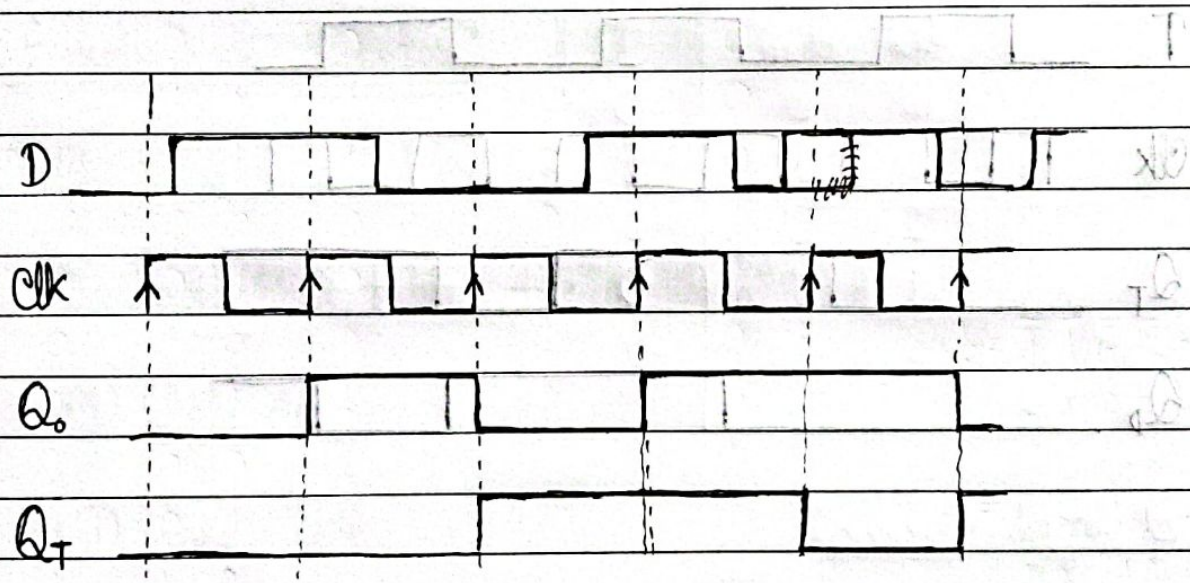
$y_3 = A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}_0$

DLD Theory-19

30/4/24

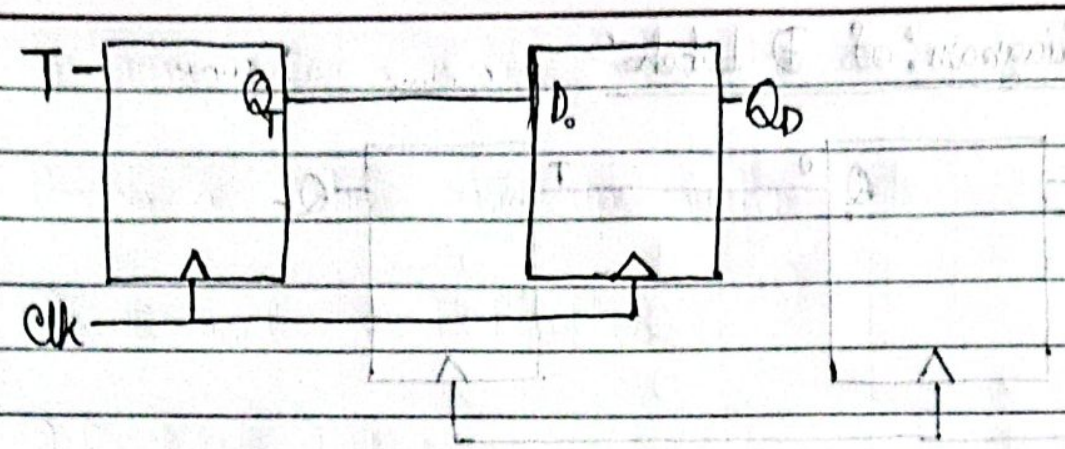
Timing diagram: of ~~D Latch~~

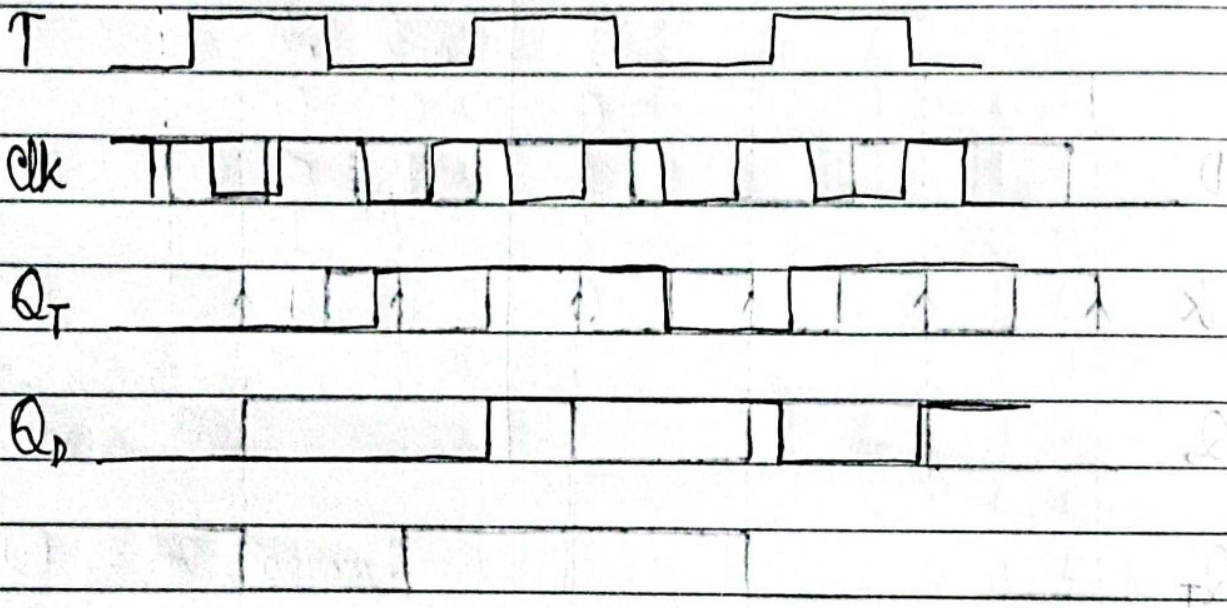




D এর আগের Output T-তে pass করবে।

#





Toggle ↳ output change হয়, আগের Output অনুযায়ী

Counter: [State counter] → Common clock pulse

* Synchronous (যেকোনো Sequence এ কাজ করতে পারে)
* Asynchronous (upword / downword এ শুধু কাজ করে)

high cost, complex design, workfast

Synchronous Counter:

1. Number of Flip Flop
2. Excitation table → opposite of truth table
3. State diagram
4. State Table
5. Function derivation with simplification
6. Logic Diagram
7. Timing Diagram

DLD Theory - 20

5/4/24

1. **Synchronous:** Common clock pulse.

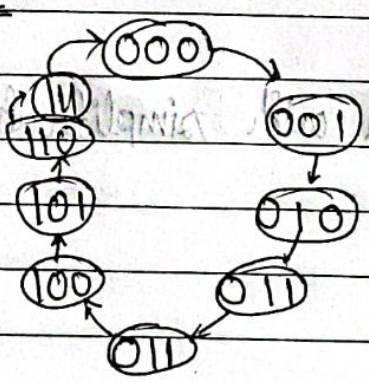
* Design a 3-bit sync up counter.

(i) we need 3 T-flipflops

(ii) **Excitation Table:**

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(iii) **State diagram:**



(iv) Stat table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

⑤ Function :

$T_0 = 1$

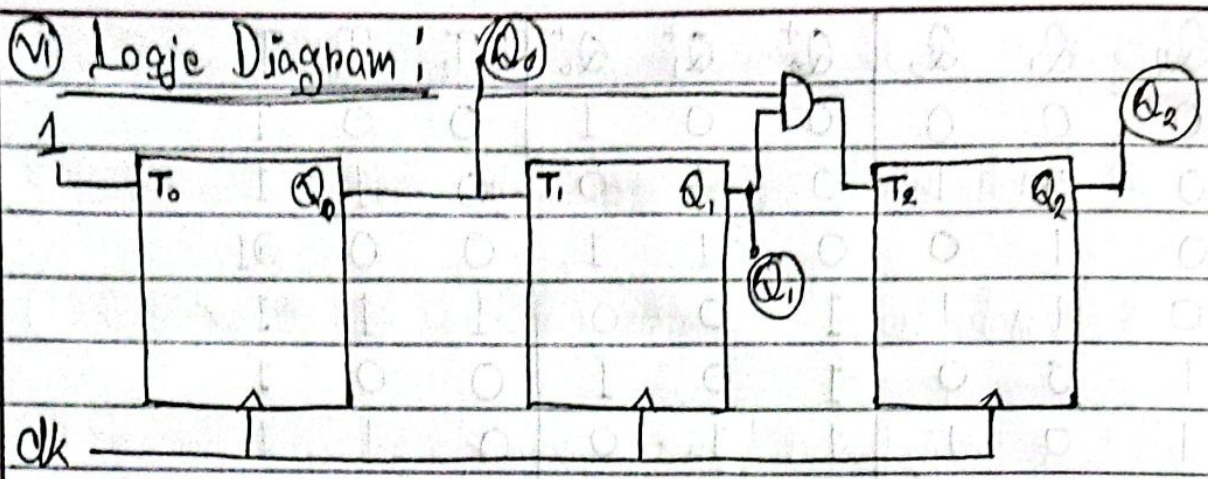
Q_2Q_1 \ Q_0	0	1
00		1
01		1
11		1
10		1

$T_1 = Q_0$

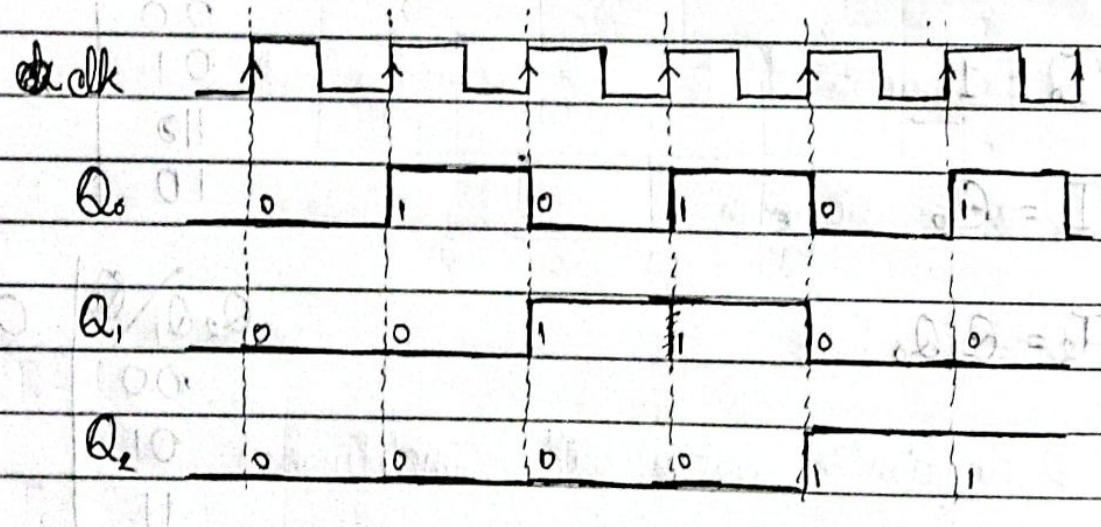
$T_2 = Q_1Q_0$

Q_2Q_1 \ Q_0	0	1
00		
01		1
11		1
10		

(vi) Logic Diagram:



(vii) Timing Diagram:



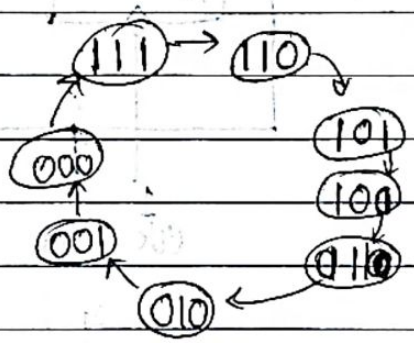
Design a 3 bit sync down counter:

(i) we need 3 flip-flop

(ii) Excitation Table:

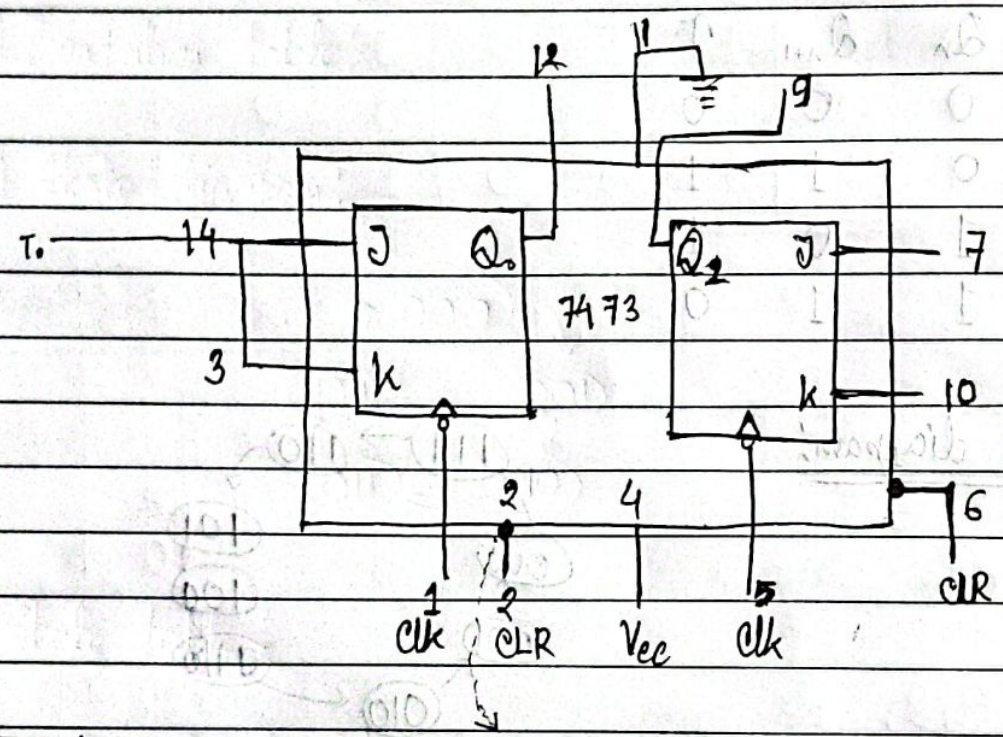
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(iii) State diagram:



(iv) State table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
1	1	1	1	1	0	0	0	1
1	1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	0	1
1	0	0	0	1	1	0	1	1
0	1	1	0	1	0	0	1	1
0	1	0	0	0	1	1	0	1
0	0	1	0	0	0	0	0	1
0	0	0	1	1	1	1	1	1



Active low

$T_0 = 1$

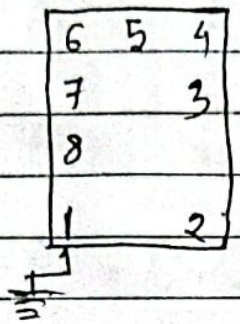
$T_1 = Q_0$

$T_2 = Q_0 Q_1$

DLD Lab - 11

12/5/24

Experiment No 10: To design a 3 bit synchronous up counter.



1 - Ground 4 - Reset

2 - Trigger 5 - Control

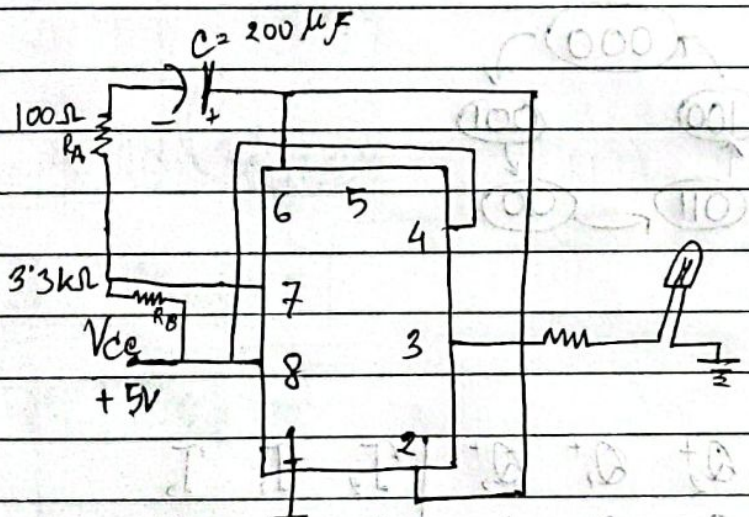
3 - Output 6 - Threshold

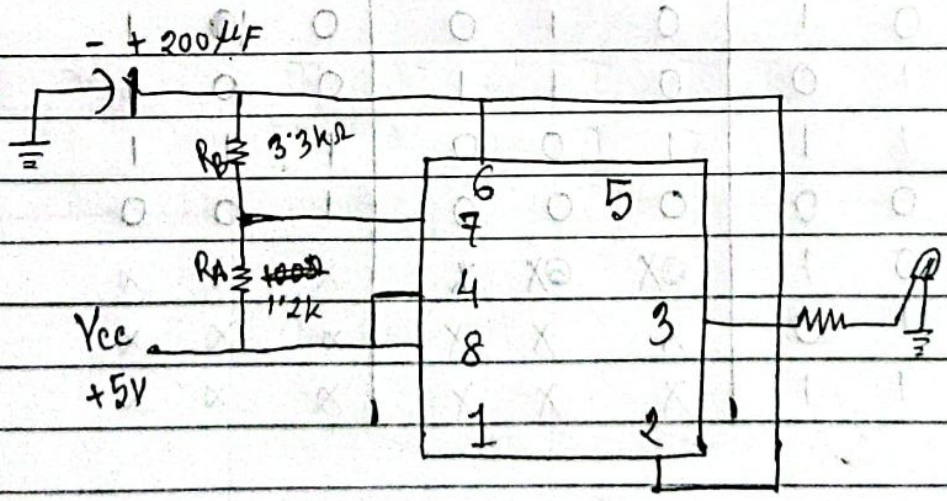
7 - Discharge 8 - Vcc.

Timer IC 555

Clk pulse

7473 JK FF





DLD Theory-21

12/5/24

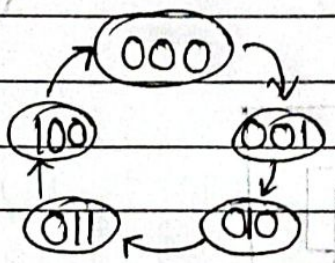
Counters:

* Design a MOD-5 ↑ (up) counter -

(i) we need 3 T-flip-flop

(ii) Excitation table:

(iii) State-diagram:



(iv) State table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	0	0
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

(v) Function:

$T_0 = \overline{Q_2}$

$T_1 = Q_0$

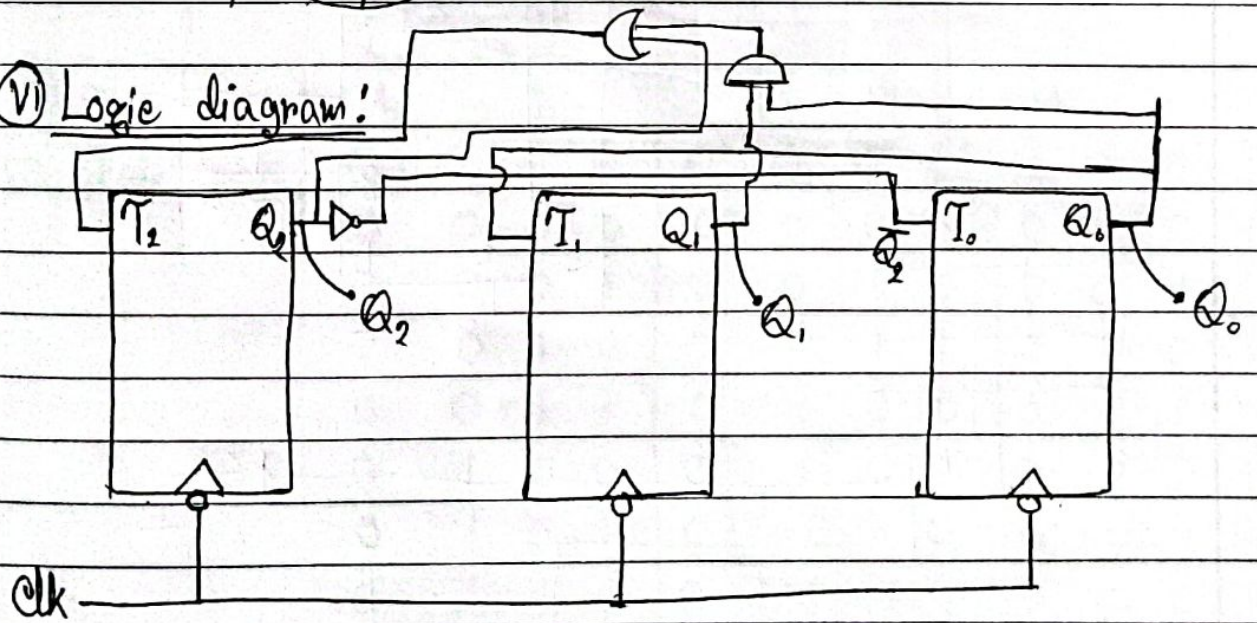
$T_2 = Q_2 + Q_1 Q_0$

Q_2Q_1 \ Q_0	0	1
00	1	1
01	1	1
11	x	x
10		x

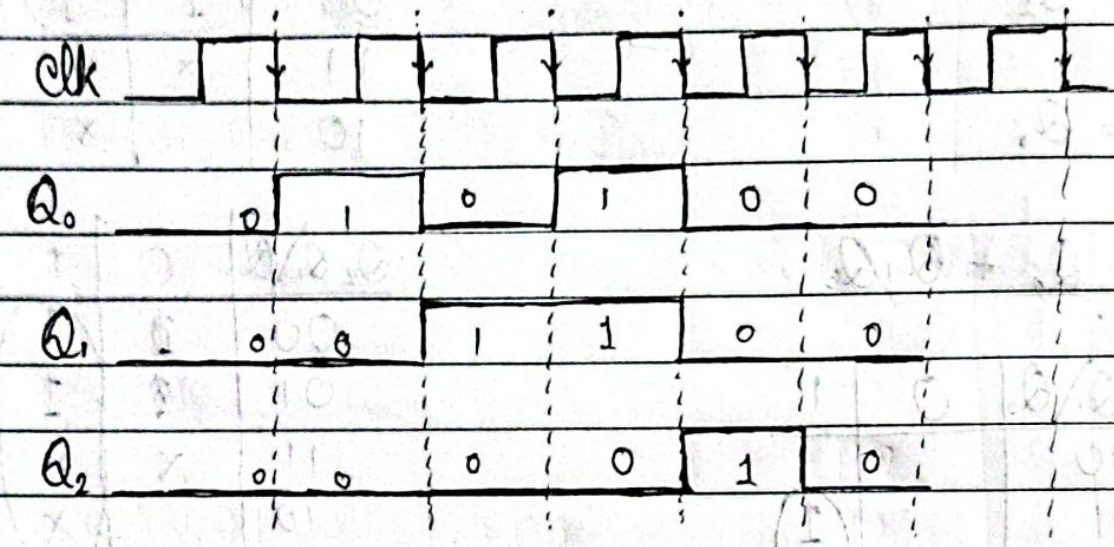
Q_2Q_1 \ Q_0	0	1
00		1
01		1
11	x	x
10	1	x

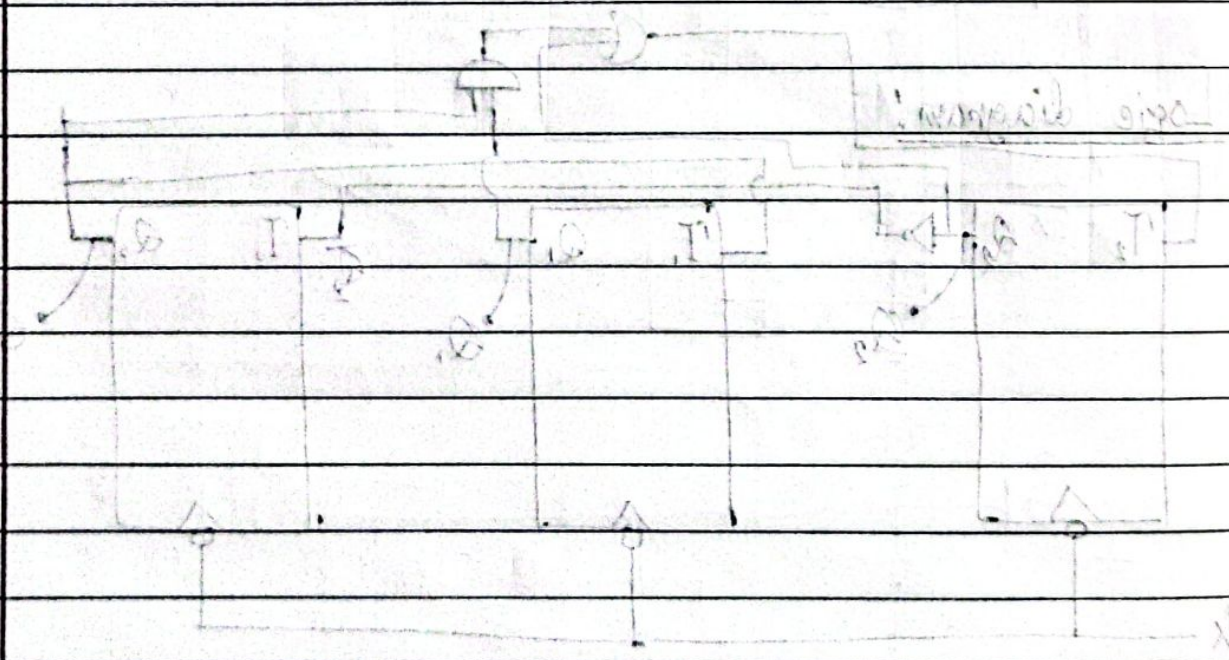
Q_2Q_1 \ Q_0	0	1
00		1
01		1
11	x	x
10		x

(vi) Logic diagram:



(vii) Timing diagram:



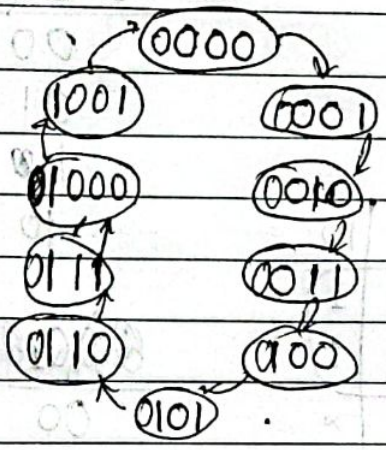


Design a MOD-10 up counter:

(i) we need 4 T. flip flop.

(ii) Excitation table:

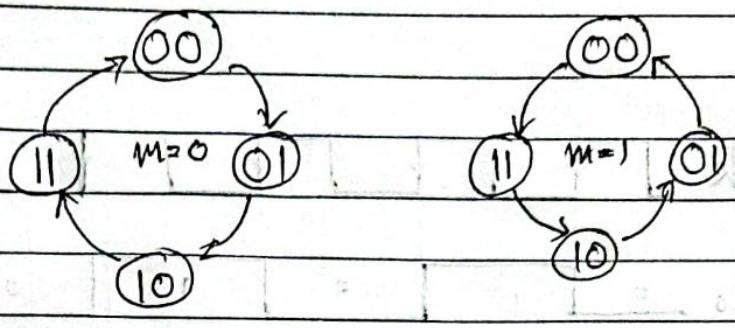
(iii) State diagram:



(iv) State table:

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0		x				x		
1	0	1	1		x				x		
1	1	0	0		x				x		
1	1	0	1		x						

Up and Down counter: 2-bit m is controller bit.



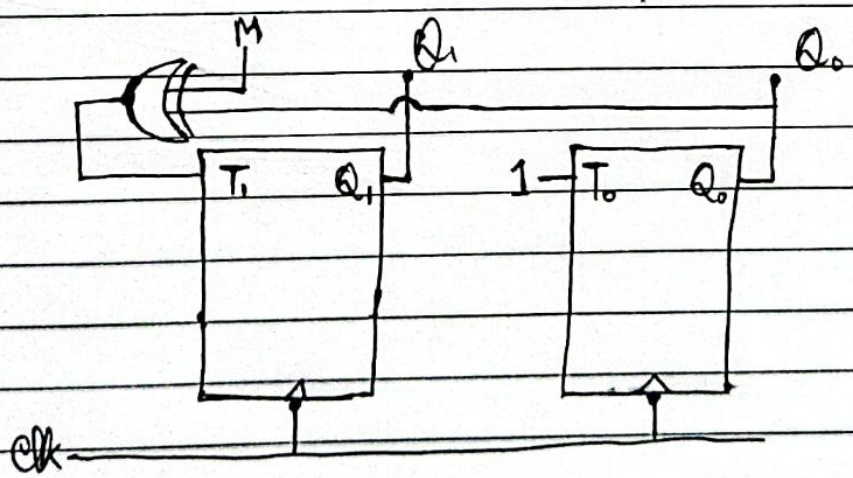
State table:

M	Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

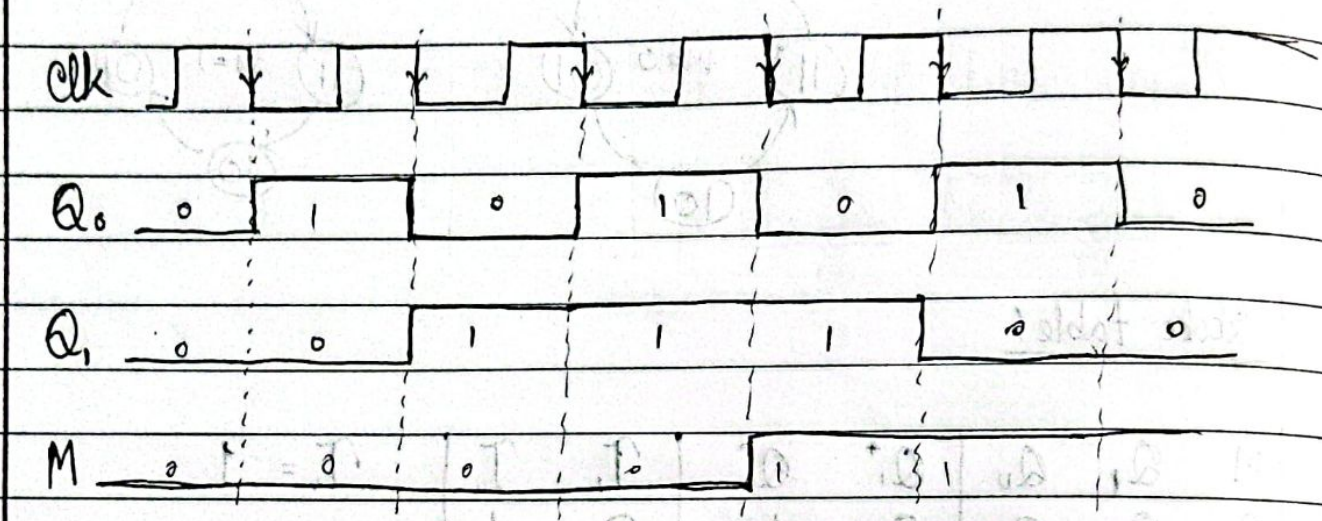
$T_0 = 1$

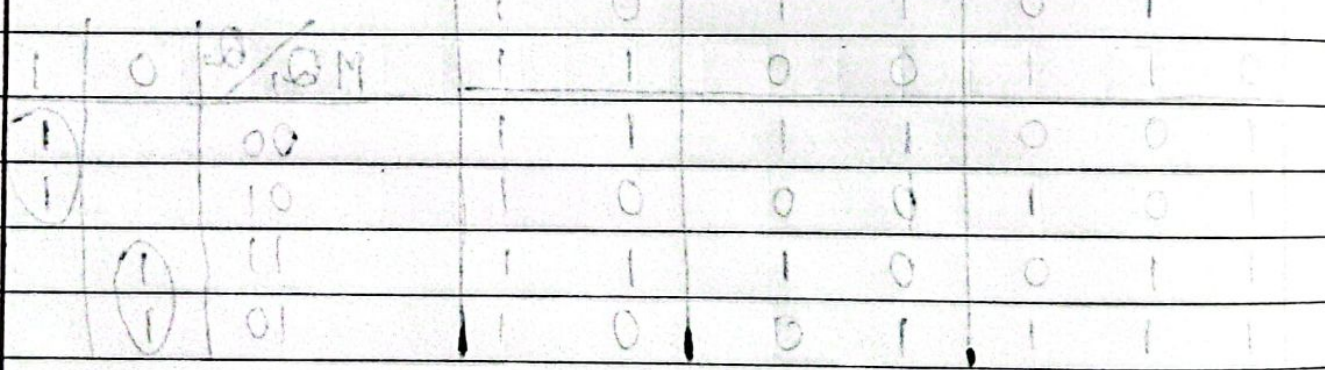
$T_1 = M\bar{Q}_0 + \bar{M}Q_0 = M \oplus Q_0$

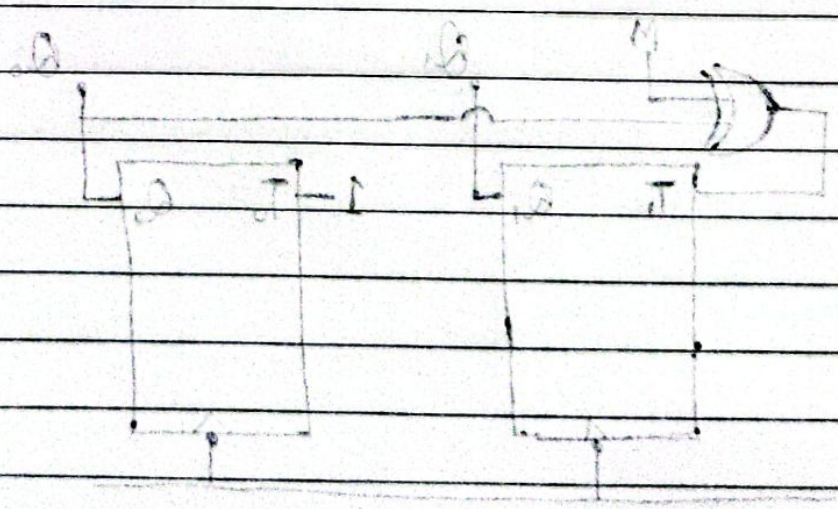
MQ_1 \ Q_0	0	1
00		1
01		1
11	1	
10	1	



Timing diagram:







DLD Theory- 23

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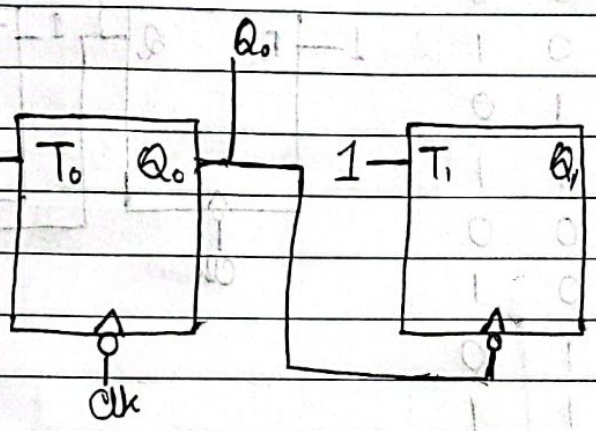
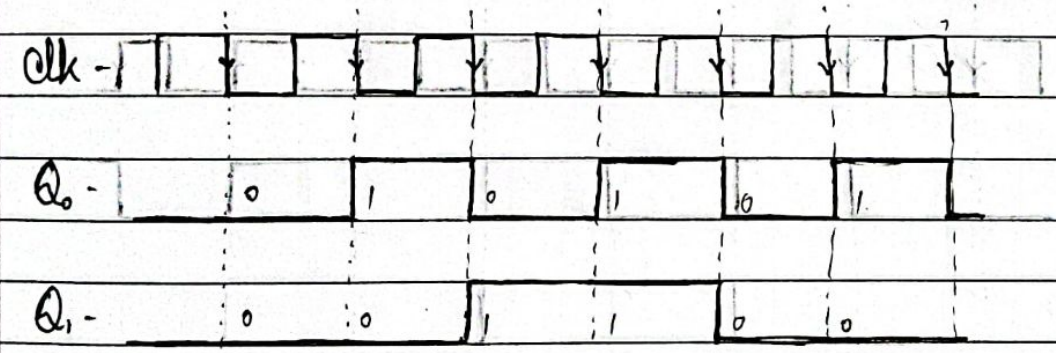
Asynchronous Counter: known as Ripple counter.

* 2 bit up counter -

Q_1	Q_0
0	0
0	1
1	0
1	1

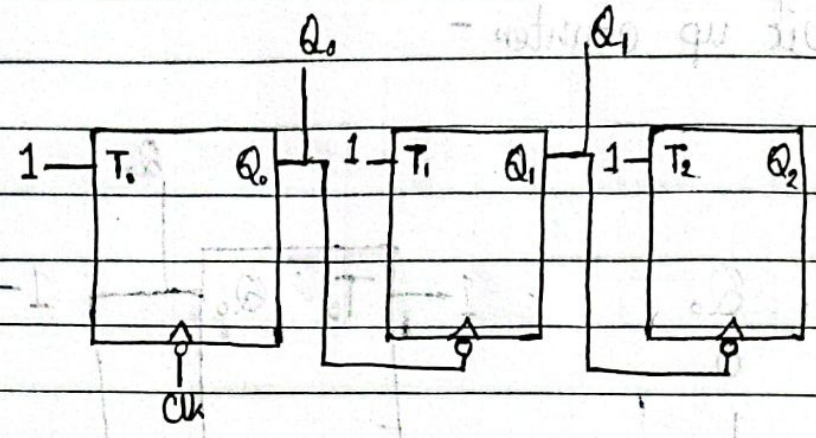


Timing diagram:

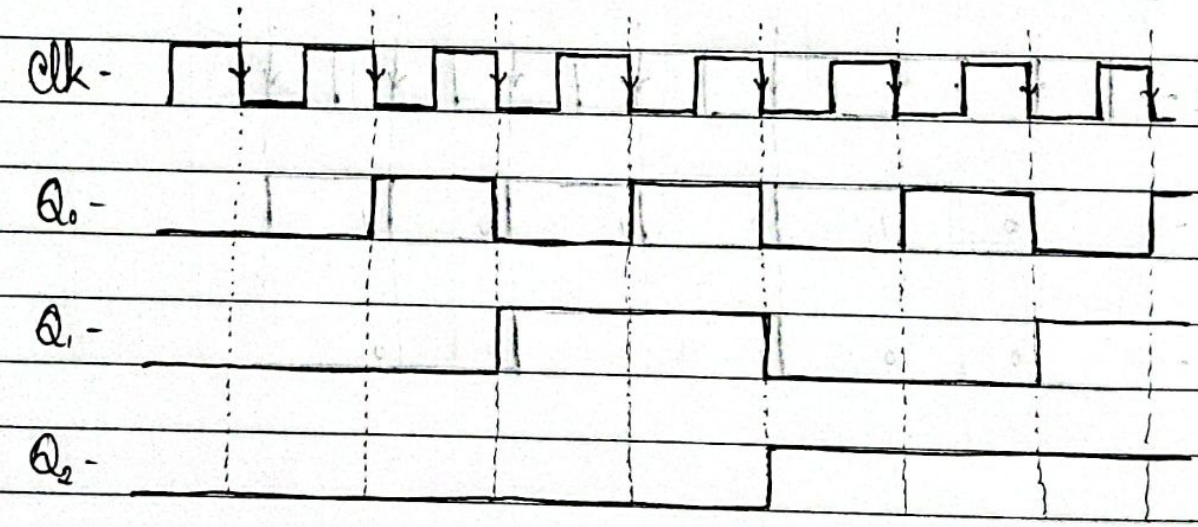


* 3 bit up counter :-

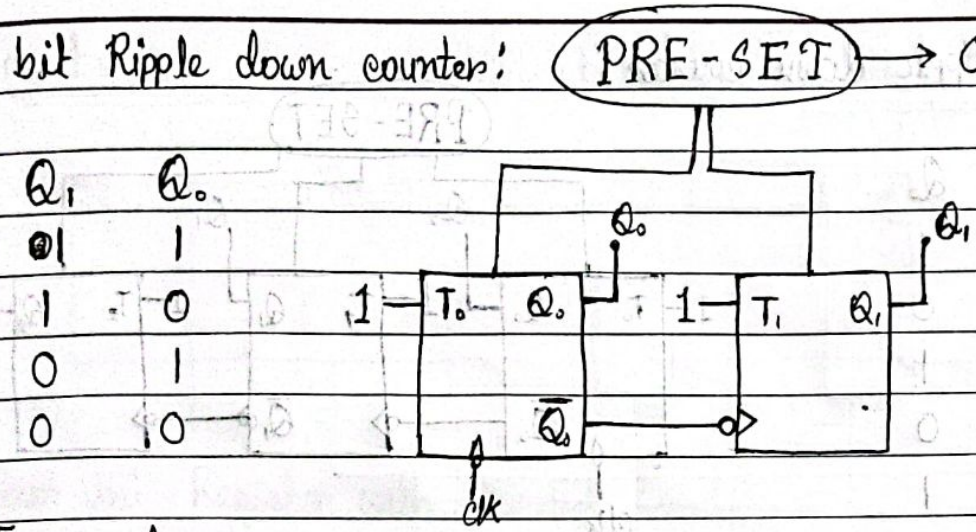
Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



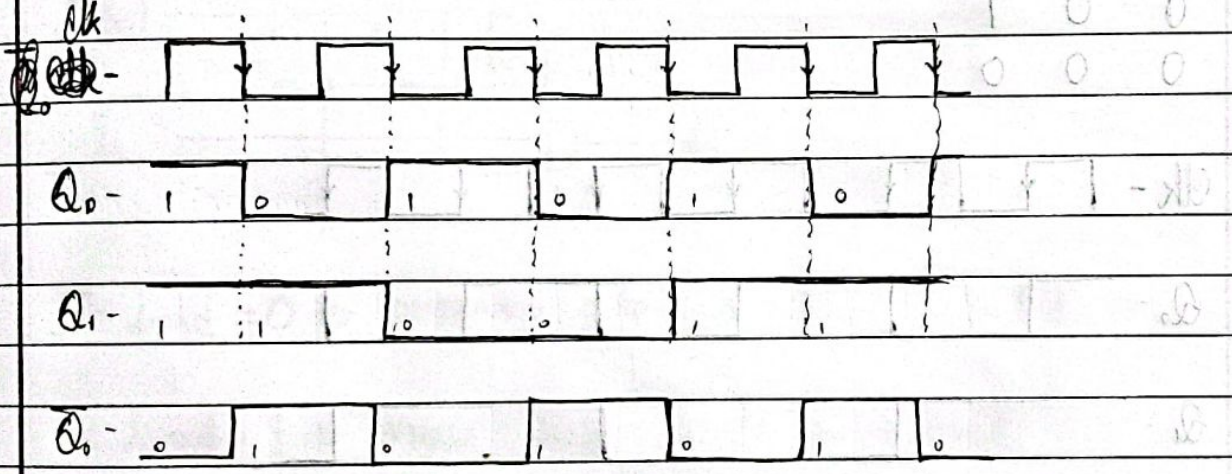
Timing diagram:



* 2 bit Ripple down counter: PRE-SET → ON

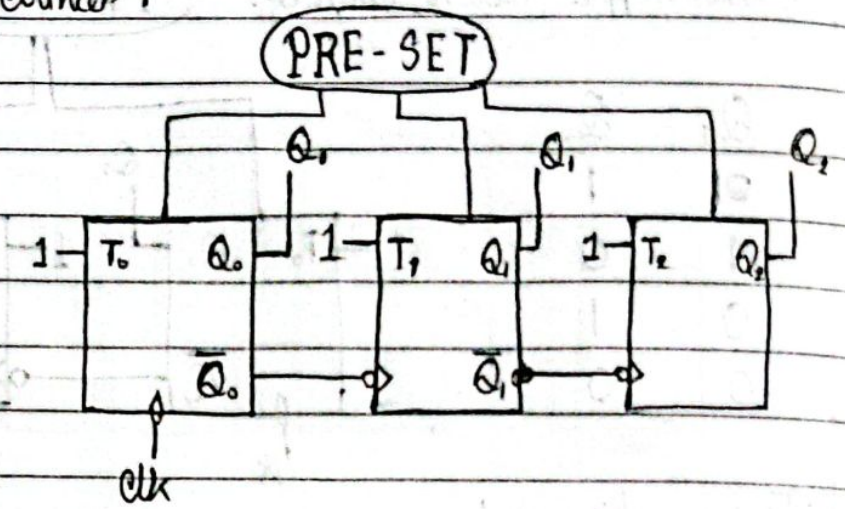


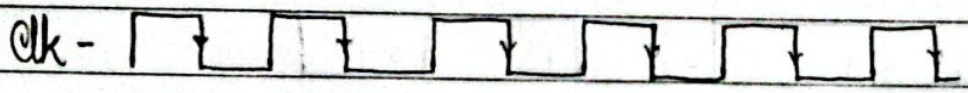
Timing diagram:

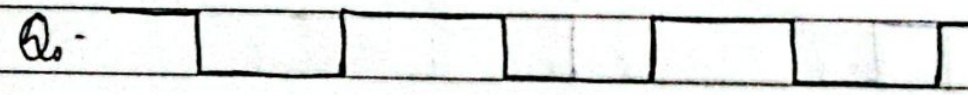


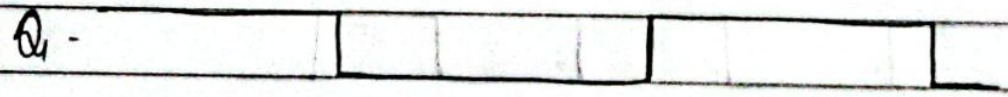
* 3 bit Ripple down counter :

Q_2	Q_1	Q_0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0









Q2 -

DLD Theory-24

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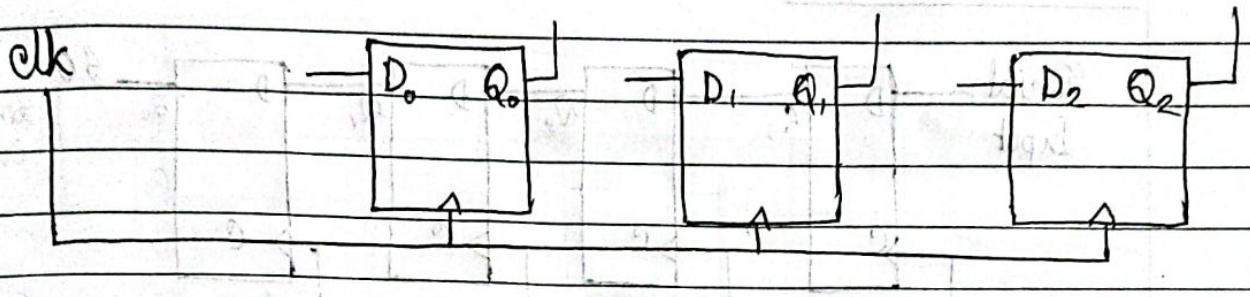
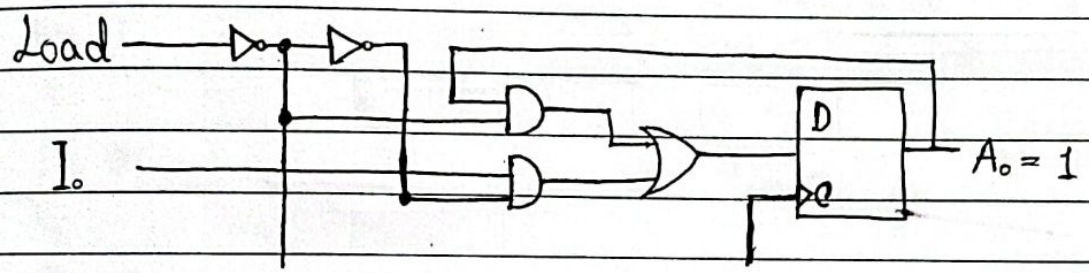
Register: Collection of D flip flop.

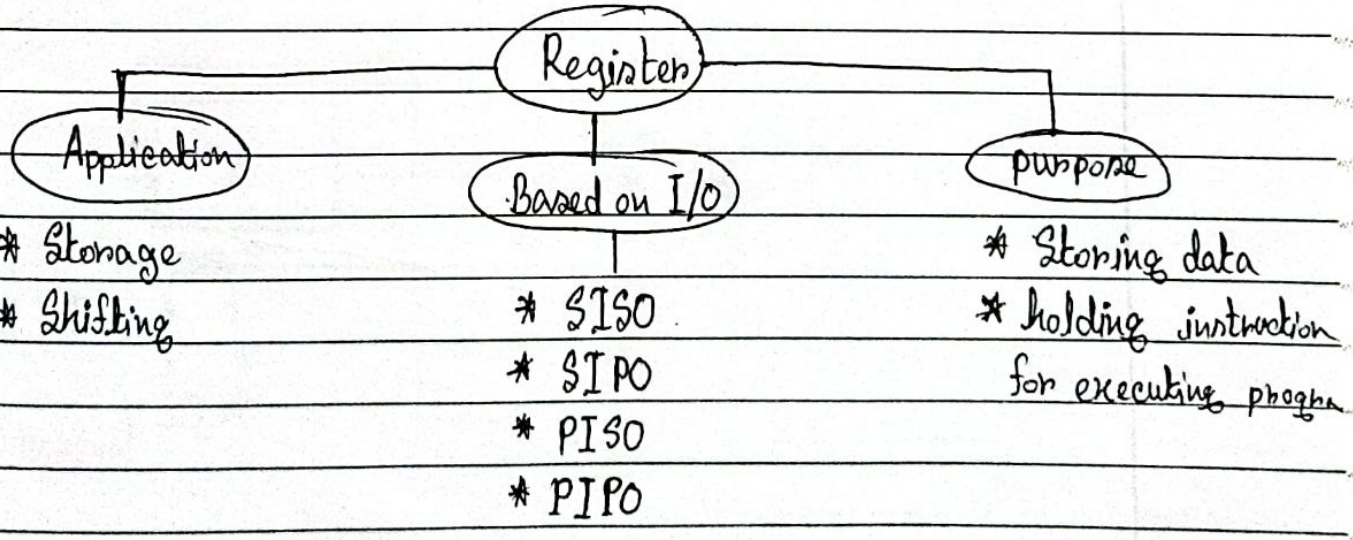


* Four bit Register with Parallel Load:

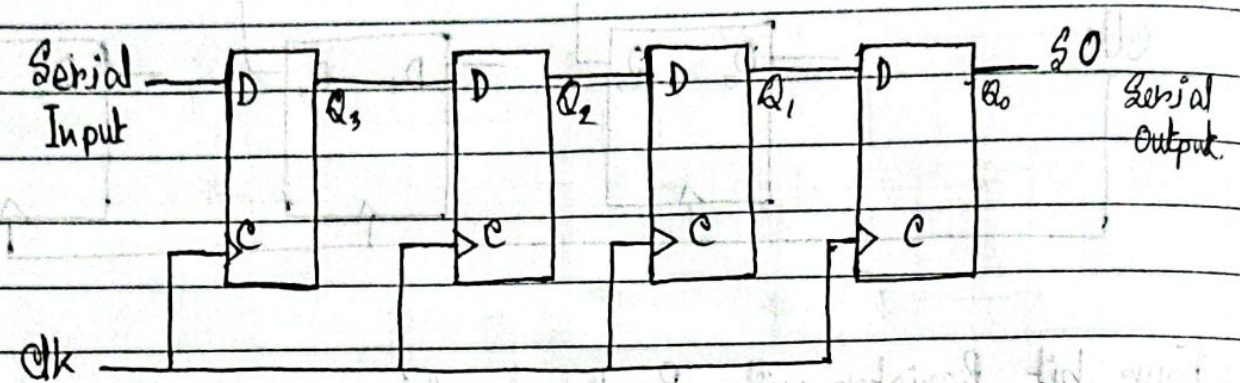


If Load = 0 ⇒ previous output should be stored.

Load = 1 ⇒ new input should be stored.



* **Shift Register:** Capable of shifting binary information



DLD Theory-25

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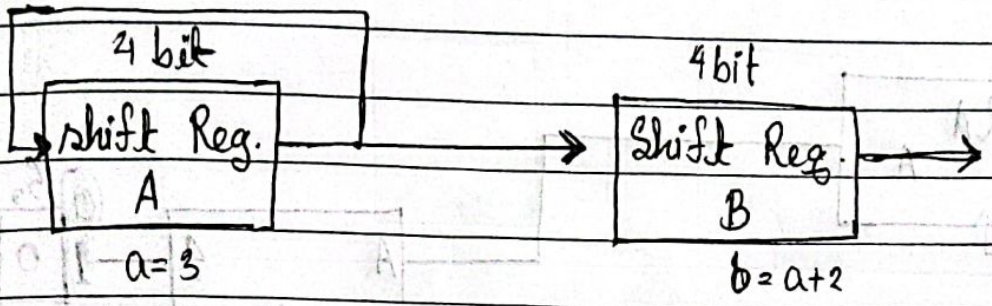
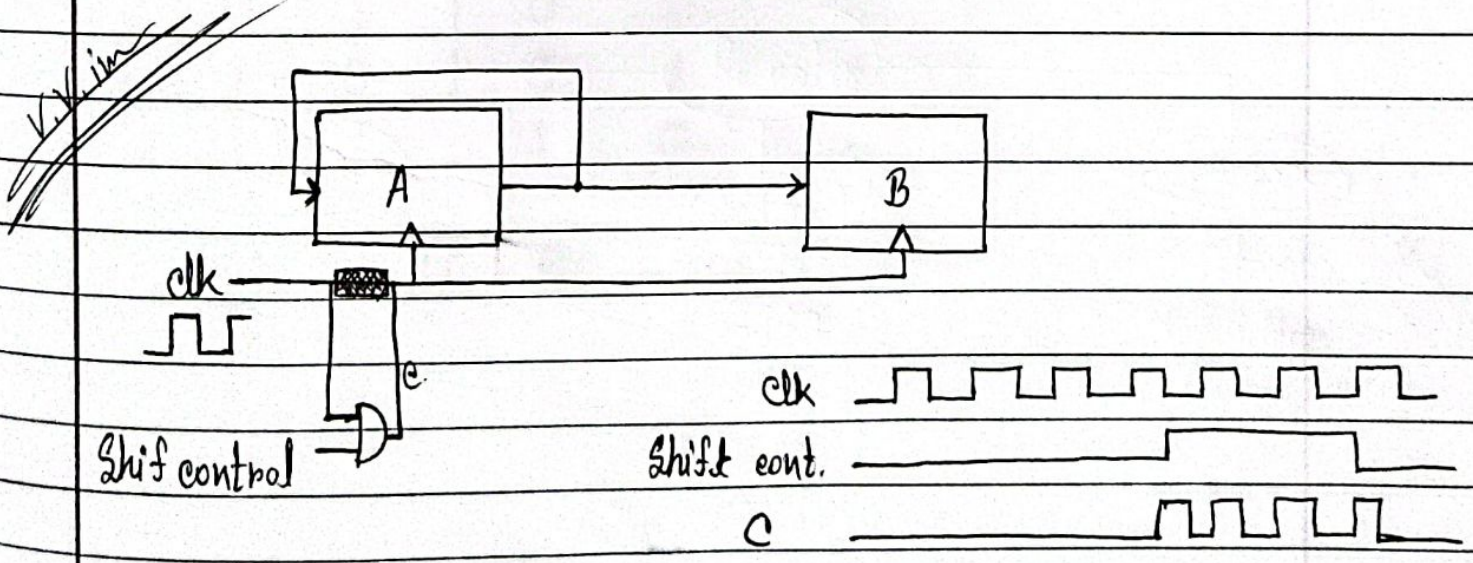
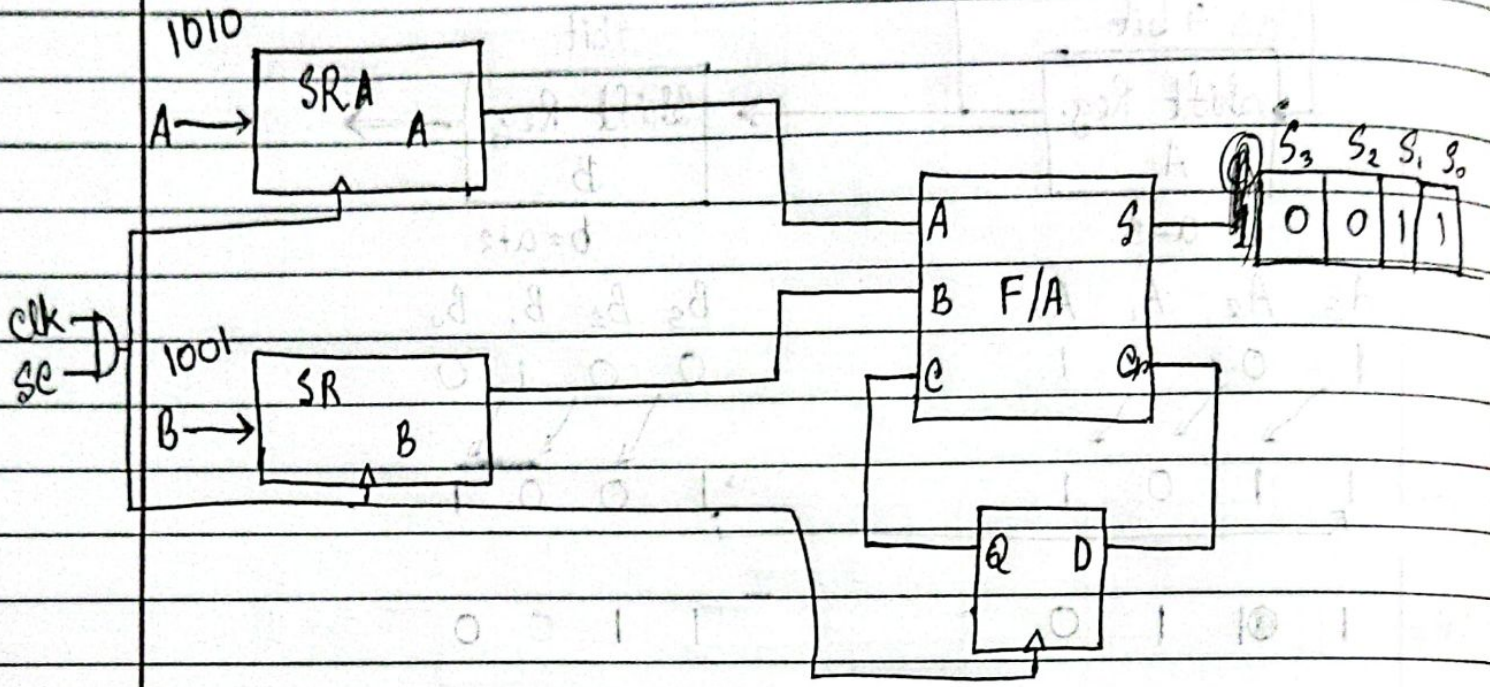
Serial Shift: shifting data from one register to another



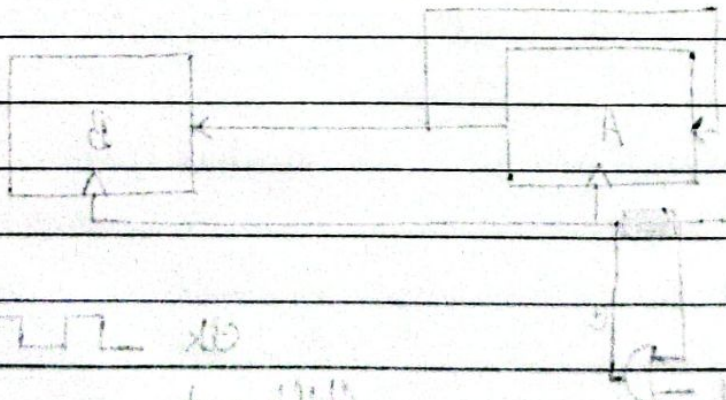
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
	1	0	1	1	0	0	1	0
1st cp	1	1	0	1	1	0	0	1
2nd cp	1	1	1	0	1	1	0	0
3rd cp	0	1	1	1	0	1	1	0
4th cp	1	0	1	1	1	0	0	1



Serial Addition: Serial Adder



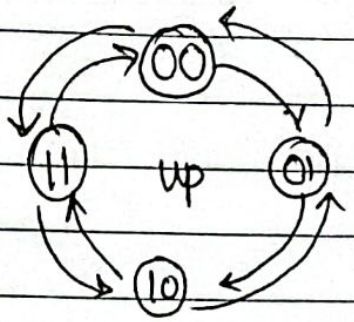
A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0		S_3	S_2	S_1	S_0
									C_3				
1	0	1	0		1	1	0	0	1	1	0	0	1	1



DLD Lab-13

2/6/24

Experiment No: 11 To design a 2-bit switch controlled sync. up & down counter.



m = 0 → up.
m = 1 → down

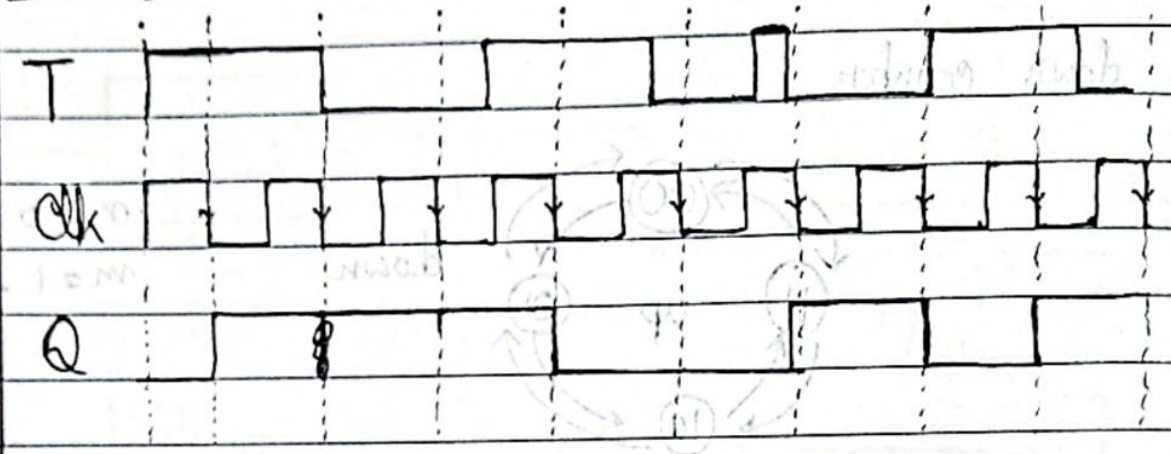
~~$Q_0 Q_1$~~ ~~$Q_1^+ Q_0^+$~~

M	Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

$T_0 = 1$ $\quad T_1 = \bar{M}Q_0 + M\bar{Q}_0 = M \oplus Q_0$

MQ_1 \ Q_0	0	1
00		1
01		1
11	1	
10	1	

Timing Diagram :



DLD Theory 26

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Design a sync counter that counts the following sequence.

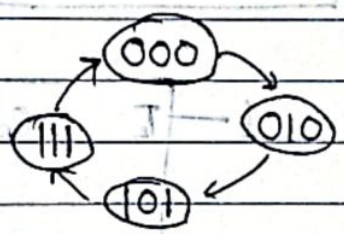
$0 \rightarrow 2 \rightarrow 5 \rightarrow 7 \rightarrow 0$

(i) we need 3 ffs.

(ii) Excitation table:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(iii) State diagram:



(iv) State table:

Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	T_A	T_B	T_C
0	0	0	0	1	0	0	1	0
0	0	1	x	x	x	x	x	x
0	1	0	1	0	1	1	1	1
0	1	1	x	x	x	x	x	x
1	0	0	x	x	x	x	x	x
1	0	1	1	1	1	0	1	0
1	1	0	x	x	x	x	x	x
1	1	1	0	0	0	1	1	1

(v) Function:

$T_A = Q_B$

$T_B = 1$

$T_C = Q_B$

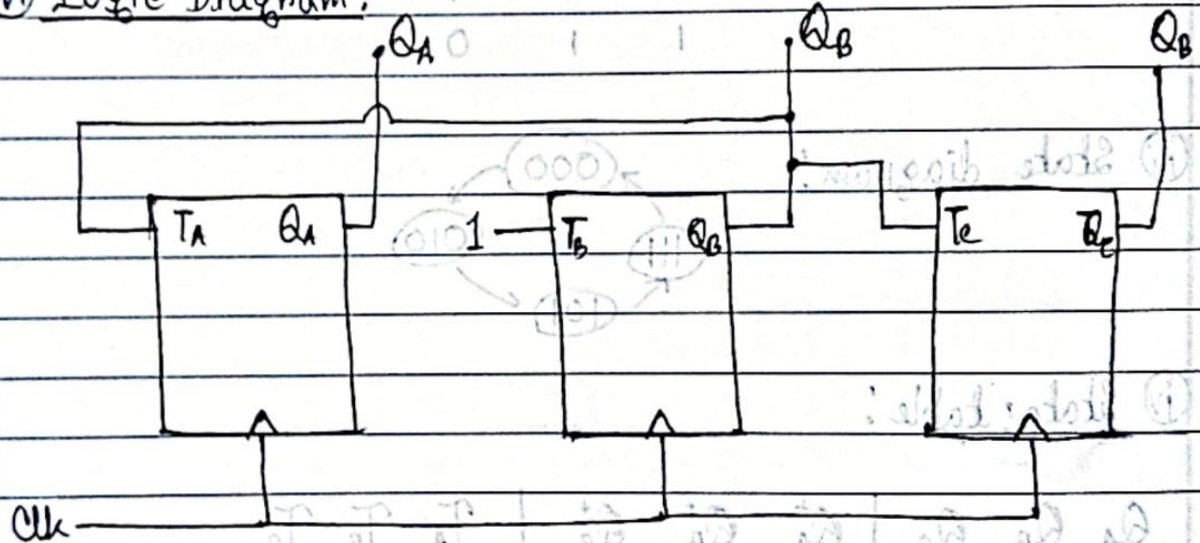
T_C

Q_A \ $Q_B Q_C$	00	01	11	10
0		X	X	1
1	X		1	X

T_A

Q_A \ $Q_B Q_C$	00	01	11	10
0		X	X	1
1			1	X

(vi) Logic Diagram:



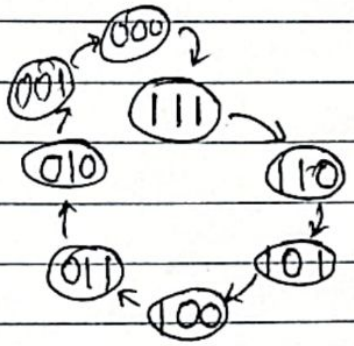
Logic Diagram

Design a 3 bit ripple down counter.

(i) we need 3 ffs.

(ii) Excitation table

(iii) State diagram :-



(iv) State table :

Q_A	Q_B	Q_C
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

(v) Logic diagram :